IN THE

Supreme Court of the United States

OCTOBER TERM 1976

No. 77-1794

AMPEREX ELECTRONIC CORP.,

Petitioner,

—v.—

THE NEW YORK RACING ASSOCIATION, INC., AUTOMATIC TOTALISATORS (U.S.A.) LTD., AUTOMATIC TOTALISATORS LTD., and PREMIER EQUIPMENT PROPRIETARY LTD.,

Respondents.

APPENDIX TO PETITION FOR WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE SECOND CIRCUIT

S. C. YUTER
122 East 42nd Street
Suite 3601
New York, N. Y. 10017
212-986-1221
Counsel for Petitioner

Of Counsel
YUTER & ROSEN
DANIEL M. ROSEN

INDEX TO APPENDIX

UNITED STATES COURT OF APPEALS

FOR THE SECOND CIRCUIT

Nos. 338, 339—September Term, 1976.

(Argued January 3, 1977   Decided April 4, 1977.)

Docket Nos. 76-7063, 76-7085

DIGITRONICS CORP., NOW AMPEREX ELECTRONIC CORP.,

Plaintiff-Appellant-Cross-Appellee,

v.

THE NEW YORK RACING ASSOCIATION, INC., AUTOMATIC TOTALISATORS (U.S.A.) LTD., AUTOMATIC TOTALISATORS LTD., and PREMIER EQUIPMENT PROPRIETARY LTD.,

Defendants-Appellees-Cross-Appellants.

Before:

MOORE, OAKES and TIMBERS,

Circuit Judges.

Appeal from judgment of the United States District Court for the Eastern District of New York, John F. Dooling, Jr., *Judge,* holding invalid for obviousness, under 35 U.S.C. § 103, United States Patent No. 3,252,149, which claims improvements in a solid state electronic system for processing data from ticket issuing machines, such as those used in racetrack totalisator systems.

Affirmed.

S. C. YUTER, New York, N.Y. (Daniel M. Rosen, Wallace E. J. Collins, and Yuter & Rosen, New York, N.Y., of counsel), *for Plaintiff-Appellant-Cross-Appellee.*

ROBERT E. ISNER, New York, N.Y. (Charles N. J. Ruggiero, and Nims, Howes, Collison & Isner, New York, N.Y., of counsel), *for Defendants-Appellees-Cross-Appellants.*

OAKES, *Circuit Judge:*

This appeal involves a patent issued for a data processing system that, when used in place of the prior art in parimutuel wagering equipment, is said to produce speedier, more accurate and more versatile paraphernalia for the placing of wagers at race tracks by those interested in the ancient and honorable art of improvement of the breed. The United States District Court for the Eastern District of New York, John F. Dooling, Jr., *Judge,* in a 216-page opinion with 52 formal findings and conclusions, supplemented by explanatory appendices, held the patent invalid for obviousness under 35 U.S.C. § 103.[1] He also held that appellees' counterclaim for attorney fees could not be sustained, since the case was not sufficiently "exceptional" to permit the discretionary award of attorney fees under 35 U.S.C. § 285. Part of the extensive opinion has been published at 187 U.S.P.Q. 602 (E.D.N.Y. 1975). On both the appeal from the judgment of invalidity and the cross-appeal from the denial of the counterclaim for attorney fees, we affirm the judgment.

Judge Dooling also found the patent invalid under 35 U.S.C. § 102 for lack of novelty and held that certain data processing systems of the appellees did not infringe the patent. In view of our agreement with the judge that the patent is obvious, we need not reach these issues.

I.

This action was brought by appellant's predecessor, Digitronics Corp., which sought an injunction and damages from the New York Racing Association, Inc., Automatic Totalisators (U.S.A.) Ltd. (ATUSA), Automatic Totalisators Ltd. (Amtote), and Premier Equipment Proprietary Ltd., for alleged infringement of U. S. Patent No. 3,252,149, issued on May 17, 1966, to Digitronics as assignee of five named inventors. The invention, according to papers filed with the Patent Office, "pertains to data processing systems and more particularly to systems for processing data received from ticket issuing machines," one of the most common of which is "a parimutuel system employed for servicing transactions or wagers made by spectators at sporting events." The patent contains 33 claims, but only claims 20-27 are in issue here. A considerable portion of Judge Dooling's opinion is devoted to developing for the reader a reasonably simplified, albeit unavoidably difficult to follow, primer of knowledge regarding the data processing circuitry and "logic" here involved, including, *inter alia,* explanations of the meaning and operation of the components used.[2] The patent itself frequently refers to

2 The judge, for example, explained that one such component, a "memory" core, contains a very large number of tiny "toroids", each of which has the capacity to represent a one or a zero (a binary number system) and in turn represents part of the numerically encoded information that is in "storage" or is being brought out of "storage." He referred to the "address" of the information in storage in the "memory" and discussed how each toroid is individually accessible to wire-conveyed impulses that impress upon it a clockwise or counterclockwise magnetic field and give it thereby a significance of one or zero. To read out the meaning, a current is applied that alters the polarity of magnetization if the toroid is in one state but not if it is in the other state, thus extracting the "bit" of information from the toroid. The judge explicated also how sections of the memory may store instructions, duly coded in binary numerical form, to govern the steps in the functioning of the device, so that the machine literally operates upon itself. And he ex-

R. K. Richards, *Arithmetic Operations in Digital Computers* (1955), which discloses many of the fundamentals of computer logic applicable in the field of data processing generally.

The patent is entitled a patent on a "Data Processing System," and each of the claims in question is one for a "system comprising" a plurality of ticket issuing machines (TIMs) or a TIM followed by a combination of particular means. As Judge Dooling found, the system is primarily an aggregator system, aggregating the number of wagers placed on each entry in two separate aggregators: the central memory register, which aggregates the wagers on each horse in each of the pools, and the TIM aggregator, where the number of wagers at that particular TIM on each horse in each of the pools is similarly (and simultaneously) aggregated. These are updated by a "unit adder" every time an additional wager is registered by any TIM. The computer draws from the central memory register the total wagers in each of the three pools and on each horse in the pool and uses those sums to compute the odds on each entry and to feed to the output display boards the results of the odds changes every 70 seconds. While elaborate circuitry is required to accomplish this, the circuitry itself is unimportant for our purposes; Judge Dooling's finding, that "there is no novel circuitry involved as is clear from the face of the patent and from the trial evidence," is not disputed here.

Appellant characterized below the subject of Claims 20 through 22 as the "totalisator system" invention, Claim 23 as the "nonallowed runner subsystem" invention, Claims 24 and 25 as the "TIM scanning subsystem" invention, and

---

plained how each toroid is wired with two "impulse" wires and one "inhibit" wire, the last to prevent the loss of information stored upon "reading" the "bit."

Claims 26 and 27 as the "erroneous data subsystem" invention. Claim 20 consists of the combination of a plurality of conventional TIMs, means of collecting from them and dispatching into the system the betting data on each entry and identifying those data to the original TIM, and means of aggregating the wagering data and sending an acknowledgment signal to the TIM so that it will stamp up and issue a ticket to the bettor with the wagering data on it. The system is composed of a set of commercially available, fairly standardized TIMs, an electronic linkage between them, an aggregator, a unit adder, and an "acknowledgment signal amplifier" between the unit adder and the TIM so that aggregating the wager effects an electromechanical release of the betting ticket. The purpose of the system is to aggregate wagers without losing track of the horse on which and the pool in which the wager was placed or the TIM at which the wager was placed. Judge Dooling found that each component was common in the prior art, existing in various forms, and performed its familiar role in a familiar way, all as basically described in Richards, *Arithmetic Operations in Digital Computers, supra.*

As to Claim 21, the court found that it added nothing to the combination, merely particularizing Claim 20. 187 U.S.P.Q. at 624. Claim 22, the court below found, like Claim 21, furnished particulars of Claim 20, adding the circumstance that the data passes from the "storage address generator" so as also to register simultaneously in the TIM memory. Put another way, the same data was being accumulated in the memory of each TIM as to that machine as well as in the central memory register. Judge Dooling found that Claim 22 really disclosed that the TIM memory and its immediately associated components are simply a conventional memory and unit adder used as a simple aggregator.

Claim 23, the "scratch" subsystem, is independent of Claim 20, and prevents betting on a "scratched" or withdrawn horse by using "a conventional equality comparator" to generate a "scratch signal" in the TIM and to prevent the TIM from operating to produce a ticket, "stepping" the "scan" to the next TIM. Put another way, a switch device emits a set of steady scratch signals and a comparison device matches those scratch signals with signals for attempted wagers on scratched entries, resulting in a rejection signal to the TIM. Judge Dooling found this not to go beyond "the obvious teaching of the use of a comparator" as a guard against taking wagers on scratches. As he said, a "comparator" exists to compare signals for identity or differences in a variety of ways, some of which can be gleaned from British Patent 749,836, cited by the Patent Office below.

Claim 24 was outlined by the patentee with reference to TIM scanning when no wagering transaction was being conducted at the TIM. Claim 24 and its dependent claim, Claim 25 (involving the converse situation where a transaction *was* being conducted or sought to be conducted) are the only ones of the claims in issue in which the plurality of TIMs is particularly significant to the claim. The object of the system is to provide a high-speed scanning means for interrogating a plurality of relatively slow operating TIMs. According to the patent itself, even absent a finding by the court below, the device which does the scanning—the "scan counter"—is a "chain of conventional cascaded binary counters," as discussed in Richards' *Arithmetic Operations in Digital Computers, supra.* The output of the scan counter is fed to the "scanner," which decodes the data from the scan counter and feeds it to the "interface" of the TIM. When depressed, the keys of the TIMs close switches, and when this is not done the scanner "steps" along to the

next TIM or, if a key for a scratched or other wrong entry has been depressed, "the scratch circuitry" previously outlined (Claim 23) "steps" the scan to the next TIM. But when a wager has been processed and error-tested the depressed wager key is unlatched, and the bet ticket is printed and issued to the bettor. Judge Dooling found that the subsystem claim combined conventional components to perform a familiar assignment in a conventional way. Both the binary counter and the scanner themselves being conventional in data processing, the circuitry he found to be "pedestrian," with a very simple goal of furnishing a pulse tracking through a system and on completion to origin ticking a binary counter.

Dependent Claim 25, Judge Dooling found, added nothing, simply covering the alternative that a wager had been made. In that case, as we have said, there is no "step," and the "selected entry transaction" signal is simply processed. The claim covers delaying the stepping of the scan over the transacting TIM to the next TIM until the selected transaction signal is checked out or confirmed and permitted to proceed. Judge Dooling found this to be "detailed and uninspired circuitry doing the routine routinely," "not even approaching the versatility of [a prior patent known as] Schrimpf No. 3029414."

Claims 26 and 27 parallel Claim 23 in that their purpose is to constitute error checks incorporated in the total device. Judge Dooling found both claims to consist of "painstaking articulation of familiar means to perform simple error checks through use of circuitry suggested by the nature of the task to be performed and the nature of the conventionally appropriate components that the tasks themselves pointed out."

The findings as to these seven claims formed the basis for Judge Dooling's decision that the patent was obvious. We, of course, may not disturb those findings unless we

find them to be "clearly erroneous." Fed. R. Civ. P. 52(a). With regard to obviousness, the statute establishes a legal standard relating to whether

> the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

35 U.S.C. § 103. We are to apply this statute by first assessing the scope of the prior art and then determining whether an ordinarily skilled worker conversant with it would think appellant's claims obvious in light of it. *See Graham* v. *John Deere Co.*, 383 U.S. 1, 12-17 (1966); *Hotchkiss* v. *Greenwood,* 52 U.S. (11 How.) 248, 267 (1851).

II.

Appellant's major argument on appeal is that Judge Dooling erroneously considered the prior art in data processing generally, rather than limiting his consideration to the totalisator business. It purports to find support for this theory in *Dann* v. *Johnston,* 425 U.S. 219 (1976), which held invalid for obviousness a patent claim involving an application of data processing in the banking industry. From the discussion in *Dann* of practices in that industry, appellant deduces that banking, rather than data processing generally, was held to be the relevant prior art. But central to the *Dann* Court's conclusion was one "Dirks" patent, which made a use of data processing analogous to that of the patent there in suit but was intended for use in any "large business organization," 425 U.S. at 228, not just banking. Because of the existence of the "Dirks" patent, "[t]here [was] no need to make the obviousness determination in [*Dann*] turn solely on the nature of the current use

of data processing . . . in the banking industry." *Id.* As Mr. Justice Marshall concluded:

> While computer technology is an exploding one, "[i]t is but an evenhanded application to require that those persons granted the benefit of a patent monopoly be charged with an awareness" of that technology.

Id. at 229, *quoting Graham* v. *John Deere Co., supra,* 383 U.S. at 19. Thus the relevant prior art in *Dann* was held to be that of computer technology generally rather than the art of the banking industry.

Since the analogy of this case to *Dann* is so close, we might not be amiss to decide the question of relevant prior art simply by reference to that case. But in the absence of an explicit statement on this point in *Dann,* we think it preferable to articulate the rule of law guiding our decision here. In determining the scope of the relevant prior art with which the hypothetical ordinarily skilled person must be presumed to be familiar, we hold simply that the court must look, in light of both the training of the patentee and the elements in the claimed invention which give it its novel quality, at what arts the patentee could reasonably be expected to consult in doing the inventing. *See In re Ellis,* 476 F.2d 1370 (C.C.P.A. 1973) (claimed invention of floor gratings; prior art included shoe scrapers); *In re Antle,* 444 F.2d 1168, 1171 (C.C.P.A. 1971) (claimed invention for mobile produce packing; prior art included produce preserving and plastic film wrapping); *Metallurgical International, Inc.* v. *Kawecki Berylco Industries, Inc.,* 348 F. Supp. 825, 835 (E.D. Pa. 1972) (claimed invention for pneumatically pulverizing material; prior art included sandblasting).

Here, as Judge Dooling found, the inventors were trained in data processing, not merely in totalisators. They worked

for a company that applied techniques of solid state electronic data processing to any industry which would hire them to do so. The patent was granted as a patent on a data processing system. And the elements of the invention for which novelty is claimed relate to solid state electronic data processing generally, not merely to totalisators. Thus the scope of the prior art in this case, in which the hypothetical reasonable person must be ordinarily skilled, and hence which the inventors here could reasonably be expected to have consulted, encompasses data processing generally and is not restricted to the totalisator business.[3]

III.

Once the art in which the ordinarily skilled person must be said to have knowledge is widened to include not only totalisators, but all of data processing, it is manifest that the patent claims here are obvious. They do not perform functions that differ from prior art in the totalisator business; they achieve those functions through means that, while new to the totalisator business, were well established in the wider data processing field: and the improved performance that resulted when solid-state electronic means were applied to perform the totalisator function, far from being unusual, was just what could have been predicted when those means were applied to perform that function.

A. *The Totalisator Function*

Parimutuel betting is, of course, a system of wagering for multi-entrant events, involving the accumulation of wagers in separate pools with betting odds and consequent

3 Our holding on this point diposes of appellant's subsidiary claim that the court below erred in not allowing it to examine the witness Fosse on the level of ordinary skill in the totalisator art. Since the applicable art was far broader than the totalisator business, the court was well within its discretion in barring the requested examination.

payoffs being determined by the comparative totals in such pools after deducting therefrom a predetermined percentage based upon the state's and the establishment's statutory shares of the pools. Parimutuel machines replaced bookmakers through the application of technology. ATUSA, an Australian concern, developed a practical mechanical and electromechanical totalisator in 1917, a multiple pool "tote" in 1923, and an automatic odds tote in 1927, installing its first system at Hialeah, Florida, in 1932, a system later sold to the group that formed Amtote. Amtote installed its first totalisator with a public display of betting figures accurate to the dollar in 1933 at Arlington Park in Chicago, and by 1962 it had almost monopolized the American totalisator business, although ATUSA had a few installations in the United States.

The totalisators or "totes" automatically permit the issuance of tickets to the bettors at the location of ticket issuing machines; aggregators accumulate the amounts wagered on each race and on each entry in a race for each of the available possible betting combinations (win, place or show, daily double, quinella, etc.); a scanner connects the ticket issuing machines to the aggregators; electrically operable display boards at various locations display entry, odds and payoff information, time of day, time of race, fractional times in the race and the like; checks are made for purposes of accuracy of the displayed information; a calculator determines the probable odds and payoffs; and all components are interconnected so as to provide for information transfer between the components and periodic updating and display of necessary information.

As of 1961, the time when the alleged invention here in suit began to take shape, the state of the totalisator art was epitomized by the Amtote Model 7J, in use both at Aqueduct and Roosevelt Raceway. The Model 7J involved the various functions mentioned above: its ticket issuing

machines, or TIMs, were of standardized construction and generally manufactured by an independent concern; its aggregators and scanner were electromechanical in operation and the display boards electrically operable; an analog computer was used for calculating probable odds, and a solid state electronic digital price computer for calculating payoffs. The Model 7J included provisions for automatically rejecting wagers on scratched horses and for checking input data for other errors, as well as incorporation of individual TIM devices for recording the bets made on each entry in each race so as to keep a permanent record thereof.

The principal prior totalisator art consisted of a series of patents acquired by Amtote on (a) a system including a stepping switch collector or scanner operating only on signal from the TIM (Levy, No. 2,182,875 (1939)); (b) an electromechanical system featuring a "jumping jack" collector or scanner (Levy et al., No. 2,179,698 (1939)); (c) an electromechanical and electronic tote using a vacuum tube non-binary counter and pulse commutators, with stepping "relay" aggregators (Klein, No. 2,557,384 (1951)); (d) an electromechanical tote system with multichannel adding machines (Johnston, No. 2,563,041 (1951)); (e) an analog odds computer for use as a component of a tote system (No. 2,652,977); and (f) the Lange tote system (No. 3,051,384 (Aug. 28 1962)) and its improvement (No. 3,080,114). The prior art also included a patent for an electromechanical totalisator issued to Handley (No. 2,479,681 (1949)), and its improvement (No. 2,680,561 (1954)), which was also an electromechanical patent involving aggregation of TIM data, means of picking up the wagers or sales or the "handle" of the machines, adding them by classes, performing other calculations on them, and acknowledging or confirming to the ticket issuing machine that the calculation had been made. A switch device permitted the emission of a set of steady scratch signals, and a

conventional comparator matched scratch signals with signals for attempted wagers on scratched entries, the signal circuitry effectuating a guard against taking wagers on scratches and other error checks. It is evident from the foregoing description that the patent claims here in suit are meant to perform the same function as this plethora of prior electromechanical data processing art.[4]

B. *The Solid State Electronic Means*

Appellant's contribution to the totalisator business involved simply the upgrading of a well-defined, existing data processing system by converting some components of the tote system from electromechanical to solid state electronic data processing. Specifically, Digitronics' totalisator, the First Tote, differed from prior totalisators in using electronic solid state aggregators for accumulating wagers and total amounts, an electronic scanner for sequentially connecting the ticket issuing machines to the aggregators, digital solid state computing devices for calculating probable odds and payoffs, and an electronic solid state memory for recording the bets made on each TIM.

While these devices were new to totalisators, they were not new to data processing. The court below found the testimony of appellees' expert witness, Highleyman, persuasive in this regard. Judge Dooling also mentioned six United States patents on these subjects; certain pages from a British patent on Univac; three publications (Functional

4 Judge Dooling also held that a prototype that Digitronics constructed as a testing and advertising device, before producing the fully operable "First Tote," its all-electronic totalisator, had to be considered part of the prior art. Whether this is so depends on whether the prototype was "commercially marketable" under *Timely Products Corp.* v. *Arron*, 523 F.2d 288, 302 (2d Cir. 1975). We need not decide this question, because we conclude that here the prior art apart from the prototype indicates performance of the same functions.

Description of the EDVAC, The System Organization of MOBIDIC, and Project Mercury Real-Time Computational and Data Flow System); and the standard text, Richards, *Digital Computer Components and Circuits* (1957). These together describe all of the solid state electronic means used by appellant. 187 U.S.P.Q. at 620-22. Further, Judge Dooling quoted the statement of Digitronics' chief executive officer to the effect that "there is virtually nothing in our device which has not already been incorporated in other machines which we have installed for other purposes in such companies as . . .," naming a railway and three large industrial concerns. The judge specifically found that Digitronics had previously supplied, for example, a medical access and analysis system for the Schering Drug Company "which involved the electronic scanning of a plurality of lever operable data input stations, the collection and storage of data obtained therefrom on magnetic tape units and the return of selectively generated signals to the data input stations." Thus we have here the routine seeking of business by a qualified data processing "system" house, followed by the routine application of then-current state of the art data processing technology to the updating of an existing data processing system of known and defined functional characteristics.

C. *The Predictable Result*

If the application of obvious means to an obvious function has "synergistic" results that would not be obvious to one of ordinary skill in the art, a patent still may issue. *Sakraida* v. *Ag Pro, Inc.,* 425 U.S. 273, 282 (1976); *Anderson's-Black Rock, Inc.* v. *Pavement Salvage Co.,* 396 U.S. 57, 61 (1969); *Great Atlantic & Pacific Tea Co.* v. *Supermarket Equipment Corp.,* 340 U.S. 147, 152 (1950); *Roanwell Corp.* v. *Plantronics, Inc.,* 192 U.S.P.Q. 65, 45 U.S.L.W.

3414 (U.S. Dec. 6, 1976) (White, *J.*, joined by Brennan, *J.*, dissenting from denial of certiorari). Here, however, the benefits that accrued from the replacement of electromechanical by solid state electronic means—increased accuracy, speed, compactness, flexibility, reliability, and economy—were, as Judge Dooling found, nothing more than the recognized advantages of electronic upgrading of a data processing system. Once the prior art is expanded to include all of data processing, appellant's only claim of "synergistic" results is based on its "multi-function TIM number signal generation means" (Claim 20b). But the court specifically found that this claim was nothing more than semantics, because in electronic data processing any system is energized from a common source and ordered in real time by a common step signal. Thus, once two different memories are used, here one central and one at each TIM, not to have simultaneous storage in the central memory register and in the TIM memory would require "a special ingenuity of indirection." 187 U.S.P.Q. at 632. Based as this finding is on expert testimony and voluminous prior art references, we cannot hold it clearly erroneous.

Mr. Leonard of Digitronics, Judge Dooling found, had "no doubts or reservations" as to Digitronics' ability to provide an electronic data processing system to perform the totalisator function. There was good reason for his confidence. As Judge Dooling put it:

> The demands of a racetrack parimutuel system on data processing resources are modest: the arithmetic calculations required are rudimentary; the range of input data is narrow, and the data are simple and easily translated into binary terms; no elaborated long-term memory is requisite; programming is simple and direct, and much of it is reducible to permanent wiring of system components; pre-existing electro-

> mechanical circuitry readily supplies patterns which are in considerable part directly adaptable to solid state electronic data processing; the service demands on data processing systems of a racetrack parimutuel system present no identifiable difference of technical significance from those of other multiple input situations.

187 U.S.P.Q. at 643. This finding seems compelled by the evidence. Having found that the function, means, and results of appellant's claims are fully anticipated by the prior art, we hold that they would have been obvious to one ordinarily skilled in data processing at the time the invention at issue was made.

D. *Secondary Considerations*

Perhaps foreseeing our agreement with Judge Dooling's conclusion that appellant's claims are obvious in light of the prior art, appellant argues strenuously that the true test for obviousness is not the court's evaluation of the patentee's inventiveness, but rather such objective, often called "secondary," considerations as long-felt need, immediate copying, and commercial success. Despite the persuasive advocacy of Judge Learned Hand, *Reiner* v. *I. Leon Co.*, 285 F.2d 501 (2d Cir. 1960); *Lyon* v. *Bausch & Lomb Optical Co.*, 224 F.2d 530 (2d Cir. 1955), this view does not represent current law. Any theory that "secondary" considerations must be given weight before a determination of obviousness can be made was laid to rest in *Sakraida* v. *Ag Pro, Inc., supra*, 425 U.S. at 282-83, where Mr. Justice Brennan concluded for a unanimous Court:

> Though doubtless a matter of great convenience, producing a desired result in a cheaper and faster way, and enjoying commercial success, [the invention] "did not produce a 'new or different function' . . . within the test of validity of combination patents." *Anderson's-Black Rock* v. *Pavement Co., supra*, at 60. These desirable benefits "without invention will not make patentability." *Great A & P Tea Co.* v. *Supermarket Corp.*, 340 U.S., at 153.

Accord, *Timely Products Corp.* v. *Arron*, 523 F.2d 288, 295 (2d Cir. 1975); *Julie Research Laboratories, Inc.* v. *Guildline Instruments, Inc.*, 501 F.2d 1131, 1135 (2d Cir. 1974); *Formal Fashions, Inc.* v. *Braiman Bows, Inc.*, 369 F.2d 536, 539 (2d Cir. 1966). *See also Maclaren* v. *B-I-W Group, Inc.*, 535 F.2d 1367, 1376 (2d Cir.) (citing *Julie Research* and *Formal Fashions* for proposition that objective criteria "are of distinctly secondary importance"), *cert. denied*, 45 U.S.L.W. 3416 (U.S. Dec. 6, 1976). Only in a close case, in which application of the subjective criteria of nonobviousness in 35 U.S.C. § 103 does not produce a firm conclusion, can these objective or secondary considerations be used to " 'tip the scales in favor of patentability.' " *Roanwell Corp.* v. *Plantronics, Inc., supra*, 45 U.S.L.W. at 3415 (White, *J.*, joined by Brennan, *J.*, dissenting from denial of certiorari),[5] *quoting Goodyear Tire & Rubber Co.* v. *Ray-O-Vac Co.*, 321 U.S. 275, 279 (1944). Because we hold that the claims made here are clearly obvious, we need not examine secondary considerations. *Compare U. S. Philips Corp.* v. *National Micronetics Inc.*, No. 76-7134, slip op.

---

5 In *Roanwell*, the Supreme Court was considering certiorari in a Second Circuit case. *Plantronics, Inc.* v. *Roanwell Corp.*, 403 F. Supp. 138 (S.D.N.Y. 1975), *aff'd*, 535 F.2d 1397 (2d Cir. 1976) (per curiam). The panel decision there is not inconsistent with the above analysis; the court said: "In view of the ample evidence of obviousness, plaintiff's arguments concerning secondary factors are not persuasive." 535 F.2d at 1398. It was the district court opinion, which relied on secondary considerations, with which Justices White and Brennan took issue in their dissent from denial of certiorari.

1323 (2d Cir. Jan. 12, 1977) (secondary considerations important because claim not clearly obvious).

Moreover, these secondary considerations are markedly less accurate as guides to nonobviousness in this case than might be the situation in another case. This is due to the domination of the totalisator business by one large company, Amtote. Thus any "long-felt need" for the improvement to which the Digitronics patent related, converting electro-mechanically operated totalisators into electronically operated ones, and its immediate use and commercial success do not necessarily mean that no one else could have made a similar improvement. On the contrary, it very likely was simply a reflection of the fact that the dominant company had no incentive to make the change because its former system, exemplified by the Model 7J, was good enough to dominate the market, and no one else was willing to make the needed investment further to upgrade its operation, in view of that domination. Once the improvement was introduced into the market, the dominant company, Amtote, was quick to introduce electronic tote to maintain its dominant market position.

IV.

Appellees counterclaimed for attorney fees under 35 U.S.C. § 285, which permits a discretionary award in "exceptional" cases, as where there is fraud in obtaining allowance of the patent by the Patent Office or other significant misconduct. *See Timely Products Corp.* v. *Arron, supra,* 523 F.2d at 305; *Kramer* v. *Duralite Co.,* 514 F.2d 1076 (2d Cir.) (per curiam), *cert. denied,* 423 U.S. 927 (1975); *Kahn* v. *Dynamics Corp. of America,* 508 F.2d 939, 945 (2d Cir. 1974) ("unclean hands" render case exceptional), *cert. denied,* 421 U.S. 930 (1975). Appellees argue that Digitronics at least had unclean hands, since in the

Patent Office proceeding it knew of but did not refer to the existence of the demonstrator prototype of the First Tote, *see* note 4 *supra,* or to its demonstration and attempted commercial exploitation.

But the court found as fact that there was no "conscious" participation by patentees and their draftsman, who was himself not told about the prototype and who drafted the application hurriedly (between January and March 28, 1963) in view of an intended sale or license of the patent. At another point the judge stated: "[I]t cannot be said that the case was pursued in bad faith, or was so wholly devoid of substance that plaintiff could not fairly be supposed to be proceeding in good faith." Although the court alluded rather darkly to the lack of "any satisfactory and reasonable explanation" for the disappearance of the prototype drawings and to the fact that they were "uniquely missing," reflecting "a discontinuity in the files," the court went on to conclude as a matter of law that "[i]ssuance of the patent was not procured through fraud or concealment or culpable nondisclosure," and hence that the case was not "exceptional" within 35 U.S.C. § 285. The weight of the evidence supports this conclusion.

Judgment affirmed.

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF NEW YORK
- - - - - - - - - - - - - - - - - -X

DIGITRONICS CORPORATION, NOW AMPEREX ELECTRONIC CORPORATION,

Plaintiff,

-against- 67 C 1119

THE NEW YORK RACING ASSOCIATION, INC., AUTOMATIC TOTALISATORS (U.S.A.) LTD., AUTOMATIC TOTALISATORS LTD. and PREMIER EQUIPMENT PROPRIETARY LTD.,

Defendants.

- - - - - - - - - - - - - - - - - -X

MEMORANDUM and ORDER

Appearances:

S.C. YUTER, Esq., (Messrs. YUTER & ROSEN, of Counsel for plaintiff

ROBERT E. ISNER, Esq. (Messrs.NIMS, HOWES, COLLISON & ISNER, of Counsel) for defendants.

F I L E D
in Clerk's Office
U.S. District Court E.D.N.Y.
SEPTEMBER 16, 1975

The trial of this action based on alleged infringements of Weida patent No. 3,252,149 has been long. The specification of the patent is not easy to read, the figures are not communicative, and the field of the patent at first blush appears complex. But the lengthy trial and the discursive manner of presentation have put in very nearly the whole background against which the patent can be evaluated. Now in suit are claims 20 through 27 of the 33 claims of the patent and the question of infringement, oddly, becomes very largely a question of the true nature, genuine scope and ultimate validity of the claims. If the devices accused do not infringe, it can only be because the claims, for all the seeming breadth of such claims as claim 20, must be narrowly read. The points of difference upon which non-infringement turns appear trivial unless the claims involved are so very narrowly read that practical effect escapes them; yet contracting them into an area of validity destroys their claim to unobviousness.

Nominally the patent is for improvements in a data processing system and particularly in systems for processing data received from ticket issuing machines. The patent application was largely drawn from a set of totalisator components and their linkage designed for installation at the raceway at Westbury, Roosevelt Raceway,

or the raceway at Monticello, or both. It is suggested, therefore, that the patent should be reviewed against the background of the totalisator art (Class 235-92), and that, so viewed, the argument for the validity of the present patent includes credit for extending to the totalisator field the art of the data processing field, and that the standard man of ordinary skill put up by Section 103 must therefore be the men who were and had for years been working on totalisators and in the totalisator field rather than those men who had the skills ordinary in the data processing field. Regrettably, that cannot be the case. The patent was granted as a patent on a data processing system in Class 340-172.5; it was a patent of a company which evidently worked exclusively in the electronic data processing field, and the patentees were men and women working in that field, and, in the years here in question, very naturally working in the newest branch of it, the solid state electronic data processing arts, invoking the use of transistors and other semiconductors.

I

The genesis of the patent was in the work that Digitronics undertook with and for the Roosevelt Raceway trotting track. The first contact of Digitronics with Raceway people was in the first part of 1959, and at a fairly

early date Digitronics was, after receiving a description of the parimutuel betting system then used at the raceway, prepared to and did propose a reasonably detailed specification for an essentially solid state electronic system covering the functions of a parimutuel system. The preliminary proposal presented to Roosevelt Raceways under date of May 11, 1959 (Exhibit F) helps to outline the requirements of a parimutuel system at a working racetrack, and at the same time the scope of the system which Digitronics was proposing at this relatively early date. It should however be noticed that a year earlier (Ex.74) Roosevelt Raceway had raised with American Totalisator Company (Amtote) the possibility of using "electronic computing machines and techniques now available "to increase betting time and expedite delivery of pay-off information in daily-double betting. Although the Digitronics 1959 proposal presupposed the use in the main of solid state circuitry, the proposal to use electronics in a totalisator system was at least a decade old. That is made clear from the Moerman patent, applied for in January 1948 and issued in June 1949 (No. 2,472,542); Moerman proposed the use of vacuum tubes and thyatrons; the system of his patent is far from a complete system;

moreover, apparently some kind of experimental installation was unsuccessfully tried out with Amtote participation at the Raceway in 1947 (Ex. 70). And there were patent application filings for electronic (vacuum tube) totalisators in 1945 (No. 2,557,384, Amtote; partially electronic), in 1949 (No. 2,652,977, Amtote; partially electronic; analog odds computer subsystem), in 1952 (No. 2,837,281, totalisator equipment; some solid state diodes, evidently used as rectifiers), and in 1954 (No. 2,987,250; electronic totalisator). The Digitronics 1959 proposal outlined the function of the equipment as, *One,* to issue betting tickets at each of the windows (through ticket issuing machines, referred to throughout as TIMs) on which would be printed out at the moment of issuance at least the number of the horse, the date the ticket issued, and the race for which the ticket was issued; *Two,* to gather the betting data continuously from up to 300 windows for each of 9 races and from each of up to 150 daily double windows, the TIMs to be adaptable to be assigned to win or place or show bets in any denomination by means of interchangeable plug boards; *Three,* to total all the bets on a race for up to a stated maximum number of horses entered in separate pools for win, place and show, to subtract the state's and club's share of each pool,

compute the win, etc. odds for each entry in the race, to compute the pay off for win and place and show at the end of each race, to show the totals bet at each TIM for each race, to show the daily double net pool, to compute the payoffs for every combination of first and second race winners rounded off at $0.10, to adjust the pool and odds data in the case of late scratches, and to make provision for computations in the event of ties of up to three-horse ties; *Four,* to display on a tote board every 70 seconds the totals bet in each race on each horse for each of win, place and show finishes, the tentative odds on each horse and the daily double net pool; after every race to display within five seconds of the judge's decision the exact payoffs and at the end of the first race, the possible daily double payoffs on each horse in the second race; and, *Five* to display at the central monitoring station and/or calculating room all the information covered in the computations in *Three* above.

Pages 2 through 5 of the preliminary proposal, Exhibit F, outline the components of the system visualized by the proposal; they may be compared with the greatly simplified block diagrams, Exhibits BL, BS and BT and the more specific and detailed block diagrams of the accused devices as shown in Exhibits 49 and 61, and the device

of the patent as portrayed in its Figures, and especially as outlined in heavy ink in Exhibits 14 through 16A.

The system as proposed was visualized as comprising TIMs, the data collection system, the computer and the display components. First, the ticket dispensers or ticket issuing machines — the TIMs; these would incorporate ticket rolls and a printing mechanism for imprinting the bet data on each ticket as issued. The TIMs were to be provided with interlocks to prevent erroneous or duplicative reporting of an operation, and each TIM was to have a counter to accumulate total transactions, which could be checked against the central data collection system. Second, the data collection system was to embrace interrogation of each TIM sequentially ten times a second, each TIM to respond with a standby sign if it had no transaction or with a transaction signal (when a ticket sale was occurring) which would indicate the number of the horse on which the bet was being placed, and each betting datum would be registered in "memory;" it was, further, to embrace wiring connecting each TIM to the central data collection system to carry the information elicited from each TIM as it was interrogated in turn and to convey a signal from the central station in effect to unlock the TIM to enable it to operate only

if the system and signals were in order. The central unit of the data collection system was to be the data accumulator, which was to have four principal parts, the scanner, the plugboard, the "interpreter," and the "memory," connected by appropriate miscellaneous circuitry. The scanner was continuously to send out in sequence various code combinations to interrogate the TIMs in such manner that the information collected identified the originating TIM. The scanner was to make a complete circuit of all the TIMs in one-tenth of a second. The plugboard was to make it possible to set up any of the 300 regular TIMs for win, place or show bets in any denomination. The interpreter was both to store in the "memory" data received from the TIM response wires and the plugboard and also to indicate any failure of these signals to conform to the rigid criteria of correct operation. Interpreter control of the "memory" was to provide signals to indicate when the TIM was locked because engaged in a sale, or because betting was closed for the race so that nothing would be added by error to the "memory," and a combination of signals to report to the memory a ticket sold on a particular horse, and for a particular finish position and in a particular bet denomination, the latter two elements b[illegible]

derived from the plugboard classification of the TIM. Once the bet had been registered in the memory, (or on receiving a standby signal from a TIM that had no transaction), the interpreter was to signal the TIM to "unlock." If such a signal did not follow immediately upon the scan cycle, the TIM was to "lock up." The "unlock" signal was to indicate registration of the bet (or simply to act as an added check in the case of the TIM with no transaction). The interpreter was also to make several types of checks against malfunction or erroneous betting.

The fourth element in the data accumulator was to be the memory whose function was to store information required for computations and for print-out or visual display. One section of the memory was to store the total wagers on each horse entered in the race in the appropriate win or place or show pool. A second section of the memory was to store the total for each TIM using the same dollar figures that were added to make up the pool totals for each horse. A detailed print-out of the TIM was to be automatically available.

The fourth major component comprised in the totalisator system proposed was the computer. It was to compute and recompute the odds at the completion of each scan of the TIMs and store the odds data for posting at frequent intervals. At the end of

the race the pay off was to be computed and available for posting within five seconds. The computer memory was to store the data needed for pay off results as well as other constants required to determine the odds.

The fifth major component comprised in the totalisator system was to be the display equipment. It was to exhibit the amounts bet on each horse for win, place and show, the total win, place and show pools, and the odds. The display material was to be brought up to date every 70 seconds. A local display panel was to be provided for monitoring the data before it was fed to the main display board (usually in the infield). After each race the payoffs were to be displayed as soon as they had been computed and monitored.

Discussions between Digitronics and Roosevelt Raceway continued over a protracted period and by November of 1959 the parties were talking in terms of first building a prototype or "simulator" on a small scale to demonstrate how the actual system of ticket dispensing, computation and display would function for both daily double and regular operations. A sort of specification was then prepared (Ex.94-A) and later incorporated in Ex.Ap but it dealt essentially in what the prototype would do

and show and how it would differ from the production model that was also in contemplation, and it did not give any specification of its components and system. However, enough appears from it to indicate that it was at least roughly compatible with the May 11, 1959, outline of the preliminary proposal so far as the system envisioned was concerned.

The outline for the demonstrator was included as the first of the exhibits or appendices annexed to the agreement (Ex.AP) ultimately made between Westbury Electronics Corp. and Digitronics which was under discussion from December 1959 and which was in form dated January 31, 1961 but which in fact was signed somewhat later, and after the failure of a protracted effort to secure the participation in the venture of Yonkers Raceway, Inc., "Exhibit B," (Ex.94B), incorporated in that agreement (Exhibit AP), was apparently prepared in February of 1960. Exhibit 94B visualized a 470 TIM installation about a quarter of which would be daily double TIMs. Exhibit 94B visualized a plan which would provide for a scan of each TIM four times per second. A scan sequence in terms of win, place and show by denominations was assumed, and it was planned that each TIM should be scanned even if locked and unused, the effect of such a scan being a zero accumulation.

The scanner was to feed its information into the central unit. The central memory for accumulating information was to be of two units, one to be called the "window" memory, which would accumulate the total transactions for each horse at each window, providing information to an individual high-speed printer. The second unit of the memory was the parimutuel memory which was to accumulate the betting data for each of the win, place and show pools for each of the horses (Ex. 94B, Figure 3-A). In the central unit both parimutuel calculation components would be duplicated, each computation would be done twice, and the results would be compared with a previous computation on that machine as well as the computation on the duplicate machine. In addition the data would be checked into and out of the memory. The operator of the entire machine by operating an appropriate control on the central panel could bypass any defective section of the dual machine for repair while the rest continued to operate. The "window" memory (i.e., TIM memory) would serve as an additional spare, since the amounts bet could be calculated, if need were, from the individual TIM accumulation of transactions for each post-position in each race by the betting denomination and finish-classification of

that TIM. "Exhibit B" annexed to Exhibit AP (i.e., Ex. 94-B) visualized that the basic unit for the entire machine would be the "timer unit," which was to "enable" data into and out of the memory, and cause the selection of the appropriate window machine for interrogation during the TIM scan; during the computation the timer would arrange for a different sequence of accesses to the memory, as required by the computational procedure. In the system of Ex. 94-B during a scan, as a TIM is examined, the selected horse number will include a check signal which the central unit would examine; if satisfactory, and if the resultant computation in the central unit is satisfactory, a "confirm" signal would be sent back to the TIM. Receipt of that "confirm" signal would permit the TIM to issue the betting ticket. Absent a "confirm" signal the TIM would lock up — a result that either mechanical defect or the "scratching" of a horse could precipitate.

Under the proposed system "memory" would be of the "coincident current magnetic core type." The memory arrangement would accommodate a total of 12 bits (that is a magnetic imprint on a tiny annulus), eleven to be used for data and one as a parity check. Each time a total came from the memory it was to be checked for an odd number of bits as well as for identity with

the quantity being read out of the duplicate memory. Once every 70 seconds during the constant scanning of the memory an odds computation would be performed. The bets were to be translated into dollars as the computation occurred. Since the TIMs would be identified and their denomination and win, place or show classification known, the raw storage element would be the number of bets at each TIM, but in the memory they would be grouped by their classes and as so accumulated multiplied by their appropriate dollar amounts to give the total of the pool for each finishing position.

At the end of the betting the output of the TIM memory was to control a high speed printer. This was to print-out the number of wagers at each TIM on each of the maximum of 10 horses that can be entered in a race at Roosevelt Raceway. Calculating room and infield displays were to be provided in considerable detail.

The part of Exhibit 94B (page 7, et seq.), dealing with the operation of the system, gives a clearer idea of the circuitry and its relation to the demonstrator. To initiate the betting, an operator at the central control must press the "start bet" control button and, by so doing, allow the issuance of tickets by the TIMs. Depressing the start

bet control button clears the memory and initiates the scanning of all the TIMs. (This is the initial clear signal (ICL) of the patent, which originates at the console as shown in plaintiff's Exhibit 4 which combines Figures 1A and 1B of the patent). Probable odds and money totals are displayed and the operation continues until the end-bet control button is pushed. Whenever a horse is scratched, the operator depresses the "scratch" button for that horse number, and that prevents any TIM from issuing a ticket on the scratched horse. (This is indicated in Exhibit 4 at the console in the series of SKW keys or levers which are numbered from 1 to N.) At each TIM at the end of the race, a printout of the individual horse transactions at that TIM is effected. When the winner has been determined, the control operator can press the Win button and the button for the appropriate horse (or — in the case of a dead heat — horses) and the "calculate" button; the result is to display in the calculating room the payoff on the winning horses. Similarly, the calculation and display are made for the show and place horses. A complete breakdown of the central system is backed up by the accessibility of the individual paper tapes of all transactions kept at each TIM as the wagers are made. These are fed into an offline window totalizer which is in effect a

high speed paper tape reader and an accumulation facility.

Under the "physical description" portion of Exhibit 94B, the presentation explains that electronic data gathering, calculation and control units, as well as the display and printout units, will be at the central location, and that the electronic memory and calculation circuits would be housed in ten racks, one of the racks including the plugboard, which could be arranged to determine the wager denomination and nature (as between win, place and show) of the TIMs. Scanning is to be by a central electronic scanning unit, and a control console would give the operator control of the displays and printouts; the console would include switches, buttons and associated indicators arranged for convenient operation. In addition, there are to be at the central control location (as noted above) a high speed 48 column printer to provide the printouts, earlier described; the printer would operate at 600 lines per minute; a pair of lister type printers would provide a 10 column, 3 line per second printout. These listers could also function as standby equipment for the high speed printer above described. There would also be included a perforated-tape reader to read the tape and

cause the printout on the listers during off-line totalizing.

The presentation describes also, at page 14, the types of errors that the system would be able to detect and make provision against. It notes that two processes occur simultaneously as the system operates: first, accumulation of the number of bets at each betting denomination for each horse and in each of the win, place or show pools and, second, the accumulation of the number of bets for each horse at each TIM (the MEMA and WM of the patent). It describes a four way check on the first process consisting in performance of the process by two computing sections, each of which checks both against itself and against the other. The second process is subject to only a two way check since it does each operation twice and thus checks against itself. Tne first process is used to determine the parimutuel betting operation and cannot permit error or down time. Transient error is to be instantly detected and signalled to the operator, but the machine must automatically select the section which is providing the correct answer and establish the correct answer in both of the duplicating sections. Hence, a transient error, it is provided, might be detected and corrected by the computer and thus be classed as a detected and corrected error. If in the first of

the two processes one side fails to operate at all, it would report "error" to the operator and could be taken out of action by operator intervention. Such an event is described as an "outage" error. During such an outage the parimutuel section will be operating essentially on the same basis as the TIM sections, that is, it will do each calculation twice and check the second result against the first. Any detected error is reported in detail to the operator while the TIM scanning process continues. Detected and reported errors take the shape of printouts on the lister of the TIM and horse number involved in the error. Since an error transaction is never entered in the totalizing memory, a TIM with a defective machine can continually report defective data which will not be acceptable to the computer, and such a window will be automatically locked up at each scan regardless of the ticket seller's efforts. This type of error would be classed as a "window-lockup" error.

Exhibit AP was not actually signed until over a year after its Exhibits A and B (Exhibits 94A and 94B respectively in the present suit) were prepared. Meanwhile there was a protracted effort to bring Yonkers Raceway into the transaction and a good deal of discussion within Roosevelt

Raceway's organization about how to handle the Amtote situation. The Raceway contract with Amtote was to expire at the end of the 1960 racing season, and Roosevelt Raceway was anxious to change that relation materially. At the same time that Roosevelt was considering trying to work out radical changes in its relation with Amtote, it was exploring the possibility of an arrangement with Western Totalizator Company, apparently a subsidiary of American Dryer Corporation and identified with Joseph Lease as its principal negotiator and perhaps a principal in the firm. At the same time, negotiations with Digitronics were pushed along in the general framework of spending something like $100,000 for a prototype to be followed by a complete installation at a cost approximating $1,100,000. Roosevelt Raceway's ideas embraced, as the draft agreement indicates, a visualization that it would itself get into the totalizator providing business. Digitronics was not unaware that it was at least possible that Roosevelt Raceway was simply playing it off against Amtote, and Digitronics prepared itself in some circumstances to see whether it could not form some kind of alliance or other with Amtote, providing Amtote with electronic know-how for the modernization of its equipment and taking advantage of Amtote's position and experience as well as its specific skills and of

Amtote's access to the Bell-Punch TIMs, the TIMs successfully used by Amtote in its electromechanical installations. By late March 1960, Digitronics was becoming convinced that Roosevelt Raceway might well decide on the prototype at least, and near the end of March, 1960 Roosevelt Raceway had an experienced man in effect go over the Digitronics materials. His report approved the Exhibit 94B proposal as satisfactory for acceptance but he had criticisms of details, particularly with respect to error frequency. On March 31, 1960 the executive committee of Roosevelt Raceway was told that an investigation of Digitronics' installations at Bache & Co., Merrill Lynch, Pierce, Fenner & Smith and other brokerage firms had been made and that the installations were said to operate to complete satisfaction. It was also reported that the electrical engineer who had been hired to check up on Digitronics had discussed with Digitronics engineers "the method and system which they intend to initiate in the manufacture of the machines to be designed and offered," that he had checked on their ability to produce and their time table for completing the prototype, and that apparently he had found nothing wrong with them; it was reported to the executive committee that the

retained expert had explained the "tremendous advantages" of electronic computation, and expressed his belief that an electronic installation was capable of much greater reliability than an electrical installation. It was thought that the equipment could be installed at Roosevelt Raceway for a sum not to exceed $1,200,000, independent of the prototype, which was not to exceed $100,000 in cost; the executive committee recognized that the investment would be depreciable for tax purposes and would, in addition, eliminate the cost for commission and rental incurred with Amtote which amounted to $473,000 for 1959. In light of all this, it was recommended to the committee that the president of the Raceway be authorized to negotiate with Digitronics for the best possible terms. At the next Directors' meeting, on April 19, 1960, there was an authorization to contract with Digitronics on the basis of the proposals submitted by Digitronics; under these, Roosevelt would acquire a 47½% interest in a distributing company, Yonkers would acquire another 47½% and Digitronics the remaining 5%.

The negotiations dragged on in the contemplation that a new company, Westbury Electronics Corporation, would be the vehicle of acquisition of the electronic equipment and act as a means of entry into the

distribution of such equipment, and it was emphasized that, after the building of a prototype, and subject to its being approved by the New York Racing Commission, or by Raceway itself, there would then be an undertaking to build and complete the first totalizator by December 31, 1962 at a cost of $1,215,000. As nothing had come to a head, finally, at the last part of May, Roosevelt in effect requested Digitronics to proceed on a letter-of-intent basis (because of the importance of Digitronics's proceeding immediately to place the necessary orders for components of the prototype); in its letter to Digitronics, Roosevelt Raceway undertook to save Digitronics harmless from any liability under a contract made by Digitronics and American Electronics for the production of prototype TIMs and such other expenses as Digitronics might incur through its engineering and other work performed for the benefit of the contract and in anticipation of its execution. It was understood that the indemnity would cease and terminate upon execution of the master contract.

Evidently, work did proceed at that time. On June 1, Digitronics reported to its directors that the formal contract to be executed with Westbury Electronics Corporation was

being delayed because of difficulties encountered with Yonkers, but that Digitronics was proceeding on the basis of the letter of intent with the building of the prototype for Westbury Electronics, to be ready by December 1960. By the time of the publication of its year end report to its stockholders on June 30, 1960, Digitronics felt able to characterize the work on the Roosevelt Raceway prototype as "Among the more spectacular systems designed during the year." The prototype was described as "an electronic totalizator which should demonstrate, at greatly accelerated speeds and accuracy (and at sharply lower cost), the electronic recording and computing of bets at the harness and thoroughbred race tracks throughout the world."

It will have been noted that the letter of intent referred to the acquisition of TIMs from American Electronics, Inc.; however, Digitronics was also, through the ubiquitous Joseph Lease, put in touch with Bell Punch Company, Ltd. in London with a view to working something out to wed the TIMs of Bell Punch and the electronics of Digitronics; and work was going forward also with Taller & Cooper on the production of Hohmann TIMs (two of which were in the end used with the prototype).

While the work was going forward at

Digitronics, Joseph Lease, for Western Totalizator, continued to put forward to Roosevelt Raceway his competing equipment and to disparage Digitronics. Meanwhile, Roosevelt Raceway's efforts to negotiate effectively with Amtote had pretty much failed, and, by the end of September, Roosevelt Raceway, although encouraged by Digitronics's reports of progress with the prototype, had questions in its own mind about whether the equipment could be fully operable and able to serve the raceway by May 1961. Accordingly Roosevelt Raceway reconciled itself to negotiating the best terms it could with Amtote looking toward a five year contract with Amtote for equipment at the raceway. Still negotiations were being conducted with the Yonkers Raceway, and nominally with Digitronics, while (at the end of September) it was expected that by November 15 the prototype would be ready for demonstration.

In this period in which work was getting underway on the actual building of the prototype, after the preparation of the "Exhibit A" and "Exhibit B," (Exs. 94A, 94B) specifications annexed to the contract Exhibit AP, the work at Digitronics was under the direction of Kiehlson; the overall logic was apparently in large part, if not entirely, supplied by Shaw of Electronics.

The connection of Mr. Weida with the project at Digitronics (where it was identified as Job 4726) dates from shortly after Labor Day of 1960. Shaw was an experienced system and logic design man who had worked on one of the historic computers, the ENIAC; he had been in computer technology from the late '40s. The logic was well in hand, and Weida got a lengthy logic write-up from Shaw when the work was turned over to him; much of the construction of the prototype was complete, and much of the wiring done; it was essentially Weida's job to follow through to get operability. The equipment was complete as a first go-around, but it had certainly not been debugged. It was first powered-up in mid to late September, but it did not at once work. There was at least one specific blunder in the system as it then existed — in the odds computation and payout part — and that had to be planned around. The first demonstration of the prototype was in mid November (see Exhibits CP, 89, 89A, and AO). The first demonstration, planned for mid-November 1960, was not to include demonstrating the daily double, but only the regular betting capabilities of the prototype.

By January 18, 1961, Digitronics was taking the view that production of the

prototype was then virtually completed but that, because of the difficulties with the Taller & Cooper TIMs, the completion of which Digitronics had had to take over, costs of the prototype would be closer to $150,000 than to $100,000; it was also indicated that the anticipated cost of the first totalizator would be $1,500,000 rather than $1,215,000. At this time Digitronics was becoming impatient with the delay in signing the contract and sought to threaten Roosevelt Raceway with abandoning the transaction after delivery of and payment for the prototype; that threat was met with Roosevelt Raceway's insistence that Digitronics could not expect payment for the prototype on contract terms if it abandoned the undertaking to complete the first totalizator.

Finally, on January 30, 1961, Westbury Electronic Corp. was organized. At the same time, the Digitronics-Westbury agreement was put in substantially final form, except that it still assumed and provided for the participation of Yonkers. It was dated at January 31, 1961, and was signed by Digitronics and Westbury, although, perhaps not until some days after its date. It continued to have as its "Exhibits A" and "B", respectively, the November 1959 specification for the prototype (Ex. 94A)

and the February 1960 specification for the first totalizator (Ex. 94B). There was also prepared and ultimately signed by Westbury and Digitronics a guarantee by Westbury to Digitronics of one half of the amounts payable by Westbury under the totalizator agreement and service agreements between Westbury and Digitronics. It had been contemplated that Yonkers would also give a 50% guarantee, but with the later withdrawal of Yonkers from the matter, that portion of the agreement was stricken out.

A copy of the agreement was sent to the New York State Harness Racing Commission under date of February 12, 1961, and about February 23, 1961, Roosevelt arranged to put $150,000 into Westbury — $99,000 of it as a loan and the balance as the price for 51% of the stock — the $150,000 to be used to pay for the prototype.

The agreement of January 31, 1961, provided in paragraph 2 that Digitronics agreed "to design, manufacture, sell and deliver to Westbury, and Westbury agrees to purchase from Digitronics, a Prototype, meeting the specifications set forth in Exhibit 'A' hereto, and the First Totalizator meeting the specification set forth in Exhibit 'B' * * *." There was prepared a proposed modification of the contract which would

have altered paragraph 2 to provide that Digitronics agreed "to design and produce a Prototype meeting the specifications * * * and agrees to design, manufacture, sell and deliver to Westbury, and Westbury agrees to purchase from Digitronics, the First Totalizator, etc." Paragraph 3 of the agreement, which referred to delivery of the prototype and satisfactory completion of the acceptance test, would have been modified to strike out the reference to "delivery." Similarly in paragraph 4 a reference to delivery of the prototype would have been stricken out, leaving simply references to completing the prototype. There is no competent evidence that amendatory agreement was executed by the parties. One copy of it was, indeed, signed by the president of Digitronics, but it does not appear that Westbury ever signed it. If the agreement had any purpose, it was apparently to make the formal point that there was not a "sale" of the prototype. The prototype was, in fact, first set up and demonstrated at Digitronics. Somewhere at or about the end of March 1961, Digitronics prepared and sent to Westbury a bill for $150,000 for the prototype showing total material cost and labor charges of $158,478.31 whereof $150,000 was invoiced to Westbury. The prototype was moved to Roosevelt Raceway

in early September 1962. Demonstrations of the prototype after that date took place at Roosevelt under the supervision of Digitronics personnel. Ultimately the prototype was stored at Roosevelt Raceway and is still there. In April 1961, when Yonkers Raceway had fairly clearly retired from the transaction, Digitronics in effect took up the Yonkers share of the stock of Westbury for an agreed price of $49,000.

At the April 18, 1961 meeting of the stockholders of Roosevelt Raceway, the president of the raceway advised the stockholders that Digitronics had completed a prototype of an electronic totalizator for Roosevelt Raceway and added, "It operates to the fullest extent we would require. At the moment it is custom built." Later, in the meeting, commenting on Digitronics (and in the context of justifying the Raceway investment in Westbury) the president advised the stockholders that Digitronics "have developed an electronic totalizator that will revolutionize the tote business."

The actual payment of money into Westbury Electronic did not take place until on or about May 1, 1961; at that date formal financing agreements were executed between Digitronics and Roosevelt Raceway. About May 2, 1961 the Westbury Electronic Corp. formally opened its bank

account with Morgan Guaranty. On May 10 Westbury drew its check on Morgan Guaranty to the order of Digitronics for $149,000 apparently in payment "on account, for design, development and production" of an invoice of Digitronics dated March 31, 1961 which set up total chargeable production costs per contract of $158,478.31.

Evidently, at this time, it was recognized that the Hohmann TIM would not do, and in late May, Lease of Western Totalizator Co. undertook to send one of his used TIMs to Digitronics; he pointed out certain of its differences from the Digitronics-Hohmann TIM; these he attributed to the fact that the circuitry of the Digitronics system required the TIM sensing unit to be in constant rotation so that the circuit would be open and waiting for the next operation. He volunteered the comment that, "Your circuit, like most electronic circuits, is not likely to be patentable and follows the usual electronic computer intricacies."

At the May 26, 1961 directors' meeting of Westbury, consideration was given to the TIM question, the possible availability of Bell Punch TIMs and the alternative of using different manufacturers to make the Hohmann type TIM. At the same meeting,

Westbury considered the question of producing a totalizator system for testing and demonstration, and Haight, president both of Westbury and of Digitronics, suggested that a 100 window machine (75 regular and 25 daily double windows) be produced by Digitronics for delivery and installation at Roosevelt Raceway at the end of the spring season in 1962 when it could be vigorously tested and demonstrated to possible customers. Haight estimated the cost at $800,000 including TIMs, of which $200,000 would represent necessary development costs. Westbury resolved to place an order for such a First Totalizator (hereinafter the First Tote), the order for the TIMs to be delayed for the present. This did not fit the terms of the agreement of January 31, 1961, which contemplated that the First Tote would be manufactured and completed in accordance with Exhibit "B" (Exhibit 94B), provided the required approval had been obtained on the basis of the prototype. Obviously, the First Tote in contemplation at the May 26 meeting was not the 470 TIM installation of Exhibit "B" (Exhibit 94B) attached to Exhibit AP which was to cost not more than $1,500,000 and which was to be delivered by June 30, 1962 provided the required approvals had been given, or the First Tote ordered by not later than June 30, 1961.

In the early days of June 1961 Haight tried to interest NYRA in the electronic tote. On July 1, 1961 Alvin Weil, in his capacity as an officer of Westbury, offered to a French race-track entrepreneur a prototype demonstration and solicited an order for electronic aggregating and related equipment for parimutuel betting in France on a large scale, indicating the need for some developmental time for particular requests that went beyond the prototype, and stating that "At present we are merely attempting to prove that existing techniques now utilized in other fields, may be adapted to the needs of a multiple issuer."

On July 21, 1961 an employee of Digitronics furnished to Haight, its president and an officer of Westbury, the presentation that the employee had used in seeking to interest an Italian group in the all-electronic Totalizator. The presentation stated that the prototype had been produced and successfully demonstrated, and that the all-electronic parimutuel system consisted of a complete tote center, TIMs, and infield display board, and other remote display boards around the track, and that the tote center consisted of a scanner, aggregator, odds computer, payoff computer, tote center display panel, and printout facilities.

Describing the functioning of the system, the presentation stated that as wagers are made at the TIMs, tickets are issued by the TIMs and that, as each ticket is issued, the wager data are automatically transmitted to the tote center (including the amount of the wager, the number of the horse and the designated pool). It was stated that at the tote center the data are entered in the "memory" and checked for accuracy. The data then enter the aggregator, which accumulates all transactions, and thence go on to the odds computer. The computer, it was said, translated all transactions into dollars and calculated the probable odds. The odds computations and totals wagered on each horse in each pool are then transmitted to and displayed at the tote center display panel, the infield display board, and remote display boards around the track. At the same time, the figures are printed out on paper, including the totals wagered on each horse in each category. After each race the payoff computer calculates the payoff for win, place and show and the amounts due the state for tax and to the track for breakage. The presentation noted that all this was done electronically, "and the heart of the entire system is the tiny magnetic memory core. It is this tiny element which permits the computers and other equipment to function so rapidly, accurately and dependably." The tote center, it was said, would

cope with scratches, dead heats and other variables. The TIMs were described as specifically designed to function with an all-electronic totalizator and to perform more functions than their counterparts used in electromechanical systems. The basic function of the aggregator was described as being to accept all details of all transactions from the TIMs, and to reject unacceptable wagers, for example, an attempted wager on a scratched entry, interdicting the issuance by any TIMs of a ticket on a scratch. The aggregator accepts data from the TIMs, stores them in the magnetic memory cores, keeps all data by number of horse, denomination of wager and win or place or show pool, and duplicates the records kept at each sales window by its TIM. The computers make all required calculations including odds and daily doubles and payoff data. Accuracy in transmitting data from TIM to tote center is assured through use of a special checking code. Two computers are used to check every step in each calculation, with the totals of each computer being checked against those of the other. Each computer can also do its computations twice further to reduce the risk of error, and both computers have internal checking features.

A little later in July 1961, Auerbach, as then president of Digitronics, wrote Bell Punch Co. in London referring to his visit there in 1960 and to a discussion on that visit of the application of electronic techniques to building parimutuel equipment. The letter stated that Digitronics had constructed a prototype electronic totalizator to demonstrate the feasibility of digital electronic technique as an economical solution to race track problems. Stating that the prototype system had been demonstrated successfully to many interested groups, Auerbach said that the company had completed arrangements to sell its first 100 window system, that the system was under construction, and that Digitronics was prepared, but indisposed, to make its own TIMs. Auerbach, therefore, inquired whether Bell Punch would quote him on 100, 300 and 500 unit quantities of Bell Punch TIMs with provision for up to 15 runners, plus a second quotation on the same quantities for only 10 runners or trotters.

Meanwhile, Lynch of Roosevelt Raceway visited Aqueduct on July 28, 1961 to see the Clary solid state computer, IBM printout unit, programming arrangement, and controls for calculation procedure there in use.

The equipment was embodied, Lynch said, in a desk sized console which contained controls for the runners and for odds in connection with the infield display board. The Clary computer was being operated for exhibition purposes in parallel with the original model Burroughs computer; it differed from the Burroughs in being more compact and somewhat faster; it had simpler inputs for the race finish, and the ability to accept a "new call" in place or show finishes without recalculating the entire finish. Lynch timed the equipment at 1 minute and 25 seconds and at 1 minute and 20 seconds for two finishes; that, he said, compared with Roosevelt's best manual time of 1 minute 15 seconds; however, he thought that the Aqueduct system had much better capacity for recalculating when there was a change in calls. Lynch concluded that, while not basically much faster than the best manual showings, the automatic equipment would be consistently quicker, not so variable, and would require considerably less personnel, making possible a savings in payroll of $130.75 a day (plus fringe benefits) for a rental price of about $110 per day.

Under date of August 15, 1961, Westbury formally authorized Digitronics to go ahead with the 100 window First Tote for $800,000 or 130% of production costs, whichever was

lower. The TIM to be used in the system was to be chosen by Westbury on or before January 1, 1962.

On October 14, 1961 Alvin Weil for Westbury answered an inquiry about electronic equipment by stating that "the Totalisator system about which you inquire is in prototype and has not as yet been developed for sale." The letter continued by saying that Weil wondered about the inquiry since the system was an "extremely specialized system which would be of interest to race track operators."

Apparently, Digitronics was having difficulty arranging for satisfactory TIMs. A trip was made to Montreal, there to examine certain TIM equipment, drawings and tooling of Joly Mfg. Co. The result was a report that they apparently had neither the tooling, the drawings, nor the personnel to do a job of producing Bell Punch type TIMs. Jotted on the back of this communication was a note to the effect that Bell Punch had told Auerbach that Digitronics would buy Bell Punch TIMs directly from Amtote, which, apparently, was believed to control any distribution of Bell Punch TIMs in the United States. An approach to Amtote is reflected in a letter of January 12, 1962 (Exhibit CW) in which Digitronics

acknowledged receipt from Amtote of one Bell Punch double machine, noted the absence of certain reject mechanisms from it, and asked whether it could be purchased without the wiring and relays but with the motor, all solenoids, takeoff switches, etc. and (since it would be without those wirings) at a reduced price.

Meanwhile, and certainly in advance of February 27, 1962, when completed copies of the brochure were mailed out to Kambex Corporation in New York (Exhibit CX), Westbury had prepared a brochure entitled "Westbury Electronic Corp. presents the world's first ALL-ELECTRONIC TOTALIZATOR." The 14 page booklet was illustrated with certain pictures of the prototype taken in June 1961. Among other things, the pictures showed the Hohmann TIMs, and four cabinets opened so that their contents could be seen; the cabinets were indicated as being, from left to right, the scanner, the aggregator, the odds computer, and the payoff computer. An electronic module card was also pictured, one of the very large number of such cards used in the Totalizator. Also included were pictures of the cabinets located at the central control area closed and partly open. The equipment was said to be all-electronic parimutuel system equipment consisting of a complete tote center, TIMs, an infield tote display

board and other remote display boards around the track. The tote center was said to consist of a scanner, aggregator, odds computer, payoff computer, a tote center display panel, and printout facilities. In the all-electronic Totalizator, the brochure stated, all totalizing and calculating was accomplished with pure electronic digital solid-state equipment with no moving parts. The elements, it was said, were small and compact and utilized electronic module cards, the same as those used in rockets, satellites, and space vehicles; they offered compactness, durability and dependability, virtually never wearing out, according to the brochure. The brochure stated that although the all-electronic totalizator performed many more functions than the electromechanical system, it occupied only 1/3 the space, the use of solid-state electronic components — such as module cards, diodes, transistors and magnetic memory cores to replace large, bulky stepping switches and other electro-mechanical equipment, resulting in a much more compact system. The flow sheet of the system was described thus: As regular and daily double wagers are made at the TIMs, tickets are issued; before a ticket is issued, the transaction is automatically transmitted to the tote center, and, only when the wager has been registered, does the TIM emit the betting

ticket; the data on the wager consist of the amount of the bet, the horse's number, and the win, place or show pool to which the bet will go; in the tote center the data are entered into the fully electronic memory and are checked for accuracy. The data then go into the aggregator which accumulates all transactions. Thence the data go to the odds computer, which translates all transactions into dollars and calculates the probable odds, and this information is then transmitted to and displayed on the tote center display panel, the infield tote display board, and the remote display boards around the track. For each race, the brochure continued, there is a continuous display of the total win, place and show pools and of the individual horse totals for each pool, the display cycling every 70 seconds. Updating takes about one second to complete. After the first race, possible payoffs for the daily double are displayed. After the TIMs are closed, the information is printed out on paper, the print-out including the number of transactions for each horse in each wager category, the dollar totals wagered on each horse in each category, and the number of wagers on each horse at each TIM. At the end of each race, the payoff computer calculates the payoff; it also computes the possible daily double

payoffs, the final daily double payoff, and the amounts due to track and state, including breakage. All these operations are done electronically "and the heart of the entire system is the tiny magnetic memory core. It is this tiny element which permits the computers and other equipment to function so rapidly, accurately and dependably." The brochure explained that each TIM can, from the tote center, be redesignated so as to change it from a window of one denomination to another, or so as to render it inoperative. The tote center is also to cope with scratches, dead heats and other variables. In the case of a scratch, the tote center instructs the TIMs not to accept bets on the scratch. The operation of a single scratch button will remove the total pool involving that horse from the probable odds computation or payoff computation. The brochure continued: each TIM takes slightly more than half a second to report the details of the wager to the tote center and issue a ticket to the bettor regardless of how many wagers are being made. All machines are scanned four times every second whether the installation is small, or one of 1,000 windows. The brochure stated: in addition to reporting transactions to the tote center, a record is kept of all transactions for each race, for each TIM for each window, and that for the regular machines, a counter is

used to record the number of wagers passing through the machine in each race, and, for the daily double machines, a perforated paper tape is punched to record each transaction so that if the entire tote center is destroyed, wagering can continue, and records of all transactions can be obtained from the TIM records to permit hand calculation of the payoff. The brochure explained: the basic function of the aggregator is to accept all the details of all transactions from the TIMs; it accumulates the number of wagers in each denomination for each horse and for each finish-position pool. The data are subject to a four way check through the duplex operation where each computer checks both against itself and against the other. The aggregator accumulates the number of wagers for each horse at each TIM subject to a two way check internal to itself. The aggregator rejects unacceptable wagers — for example, a wager sought to be placed on a scratch — and does not allow the TIM to issue a ticket on such an attempted wager. As the aggregator accepts data from the TIMs, it stores the data in the magnetic memory cores; in maintaining these data, it duplicates the records kept at each window by the ticket issuing by the TIMs. The brochure stated: the basic function of the computers is to do all of the re-

quired calculations, translating them into dollars. Totals for all race wagers and probable odds are calculated instantly with the probable odds calculation being done every 70 seconds. After each race, the computers calculate the public payoff within 15 seconds after the order of finish is punched into the central control units and in the case of the daily double, in about 10 seconds. Accuracy of transmission of the data from TIM to tote center is assured through use of a special checking code, and accuracy of calculation is assured by using two computers to check each step in calculation, the results being compared to make sure they are accurate. In addition, each computer can do its own calculations twice — further to reduce the risk of error — and additional internal checking features are built in. (Exhibit U and Exhibit 120)

At the March 7, 1962 meeting of the Directors of Digitronics, Auerbach reported on the Italian totalizator situation; he indicated that preliminary talks pointed to a 10 year contract with a 2% of gross handle being Westbury's income.

At the Roosevelt Raceway stockholder's meeting of April 17, 1962, Alvin Weil, then president of Roosevelt Raceway, devoted an extended part of the meeting to discussion of Digitronics, Westbury Electronic, the

prospects of the use of completely electronic parimutuel betting at Roosevelt, and exploitation of the market for such equipment through Westbury Electronic Corp., in which Roosevelt was a majority stockholder. Apparently display cards were used at the meeting to explain the new tote system, and Mr. Weil used the familiar statement that "the heart of this equipment is a little circular thing that could lie right in the center of the palm of your hand * * *. This is the memory, this is — or a number of these, of course, is what takes together all of this information, holds it, sorts it and then puts it out when needed."

In the latter part of May and the first days of June 1962, the plans of Digitronics and Westbury Electronic Corp. took the direction of completing the First Tote as an installation of a 100 TIM system at Monticello Raceway about March 15, 1963, following a demonstration of adequacy at the Digitronics plant about February 1, 1963. The Monticello installation was to be utilized as well for taking bets at Vernon Downs and at Buffalo through some sort of long lines connection, while the control center remained at Monticello. That first installation was to be followed by the completion of a large installation at Roosevelt Raceway by March 1, 1964, and the transfer

at that time of the central control and computer units from Monticello to Westbury. It was visualized that Aqueduct, too, would be added to the system in March 1964. The whole program, it was thought, might cost as much as $4 million, and, if extended to off-track betting in New York City (provided such betting was legalized), would also include facilities for that operation at another $400,000 of cost. At this point, the cost estimates assumed Bell Punch TIMs on the first installation with Westbury Electronic TIMs to be used thereafter. The ambitious program was keyed to approval by the New York State Racing Commission of the Westbury Electronic equipment at the time of the initial demonstration at Digitronics in February 1963. Haight was in the course of going to England to negotiate with Bell Punch for 165 TIMs for use in the First Tote. To assure Bell Punch of payment, Westbury Electronic Corp.'s thin capitalization was to be supported by a Morgan Guaranty Trust Company guarantee backed up by Roosevelt Raceway. (See Exhibits 122, CZ and BE)

In early August the problem of getting hold of Bell Punch TIMs was still, as a practical matter, quite unsolved. There was discussion of maintaining pressure on Amtote to get Bell Punch TIMs from it, speculation

about the possibility of getting them from Joseph Lease via Canada, and the possibility that, at least for the hoped-for Italian installation, London might be persuaded to supply Bell Punch TIMs directly for delivery in Italy, despite the risk that they might be diverted from Italy to the United States. By the end of August, however, Digitronics was in touch with Australian Tote.

Australian Tote indicated a willingness and ability to supply 190 TIMs by the year end of 1962, and Digitronics was interested in trying to work out some arrangement with Australian Tote to supply it with electronic components for its TIMs; Australian Tote seemed to be concerned only with seeing to it that Digitronics did not copy its devices. At the same time, Australian Tote indicated that IBM wanted to discuss not only the design of Australian Tote's machines but also the buying of IBM's TIM requirements from Australian Tote.

By early September 1962, the planning, somewhat changed, was tending to be that final assembly and erection of the First Tote might be at Roosevelt (rather than Monticello). Delivery of the First Tote was scheduled for February 1963.

Still in the early part of September 1962, the negotiation with Australian Tote was

pressed, and it appeared that a satisfactory arrangement could be worked out between Digitronics and Australian Tote, starting with the loan of one machine to Digitronics, to be followed by the delivery of two unmodified machines, all three to be used with the prototype for test purposes. Beyond that, the discussion was over ordering 165 additional machines that would be modified by substituting for their standard "selector arm mechanism" a push-button system and the addition of a relay and adjustment for use with 120 volt direct current rather than 50 volt current. It was visualized that the orders for the Australian Tote TIMs would fulfill the requirements at Monticello, the deliveries being staggered between the partial requirements for the February demonstration and the complete requirements for the March installation, presumably at Monticello. At the same time, however, discussions continued with Joseph Lease for the delivery from Joly Mfg. Co. in Montreal of 200 regular and 60 quinella TIMs of the Bell Punch type, 148 of which were said already to have been assembled for another race track which had failed to complete the purchase. These were supposed to be deliverable by the end of January 1963. Digitronics wondered whether the person behind the Lease offer

might not be Bell Punch itself, acting through Lease. In any event, the negotiation with Australian Tote (which will hereafter be referred to as Atusa, indicating Automatic Totalisators (U.S.A.) Ltd.,) was proceeding to the point where, at the end of September, Digitronics and Atusa were discussing specific contract terms, and Digitronics was expressing a preference for the Atusa TIMs over the Hohmann TIMs which it had worked out with Taller & Cooper. By October 10, 1962, Westbury, and presumably Digitronics, were proceeding on the assumption that Atusa would make J10 push-button TIMs available in time for the demonstration in February 1963. One type of J10 apparently could be switched from regular to daily double betting very simply, and it was the view that only 120 machines would be needed, 40 of these to be converted to and from daily doubles operation. That circumstance, it was reckoned, would bring the cost of the Atusa TIMs within the projected budget for the project.

Amtote, apparently, had been given some sort of an order for 152 Bell Punch TIMs, but it was understood that Amtote had not unequivocally accepted the order, and Westbury determined to terminate the order for all except 13 Bell Punch machines to be delivered in October 1962. Apparently there

was also under consideration a proposed development contract with an outside firm for an on-track and off-track TIM, with, apparently, some expectation that the on-track TIM might be "more important to the February demonstration than the off-track devices."

At length, under the date of October 30, 1962, a letter agreement was signed between Westbury Electronic and Atusa covering 122 J-10 TIMs ordered for Westbury Electronic Corp. by Digitronics Corp. at a total cost of $246,226 FOB Sidney, Australia. Twenty of the machines were to be shipped not later than January 15, 1963 and 101 machines were to be shipped not later than March 31, 1963. The carrier was to be designated by Westbury (which was, of course, to pay the freight).

Meanwhile, at the beginning of November, it was, in light of certain financing which Digitronics was trying to arrange for itself, more or less agreed between Westbury and Digitronics that the January 31, 1961, agreement had become obsolete because of the later conduct of the parties, and that they needed a new agreement. However, without any new agreement, the parties were working along on the completion of the First Tote. At a meeting in

Phoenix in late November 1962, held to discuss technological advances, the contract between Atusa and Digitronics was disclosed, that the Atusa TIMs were being modified or adapted to the new Digitronics tote, and that there would be a complete display of the Digititronics Tote in mid February at Roosevelt Raceway, which all were invited to attend. The representative from the New York Racing Association (NYRA) indicated that the meeting had produced a lot of interesting talk, but nothing concrete; he stated, however, that if someone really came forward with something, NYRA would go anywhere to inspect it.

In early December 1962, Amtote was pressing Monticello to renew its Amtote contract emphasizing Amtote's improvements in its equipment over the years, including its use of solid-state or transistorized computer elements, and warning Monticello that any new device would require far more testing than non-technical people appreciated, and that this was particularly true of equipment intended for racetrack use because of the sharp contrast between laboratory or office conditions and actual operating conditions at a race track. Amtote closed by giving Monticello until December 31, 1962 to sign up for a new contract.

About the middle, or a little after the middle, of December 1962, Amtote delivered to Westbury through customs, 13 Bell Punch machines for $20,839, ten of them regular machines and three of them daily double machines.

During the year 1962 construction of the First Tote was progressing under the superintendence of the patentee, Robert L. Weida, and in December 1962 it was moved to Roosevelt Raceway. By February 12, 1963, the work was so far complete that 20 TIMs could be in use and accept bets, odds could be computed, payouts calculated and readouts set up visibly. It had already been decided that the First Tote would be given an essentially public demonstration on March 6, 7 and 8 at Roosevelt Raceway. The demonstration contemplated would, again, have used 20 TIMs and there appears to have been little doubt in the minds of the people at Digitronics that the demonstration would be successful. For example, in a letter written on February 12, 1963, to a London insurance broker, Westbury or Digitronics, or both, expressed interest in finding out whether they could offer, with the Totalizators that they were to market, insurance against losses incurred through breakdowns in the electronic Totalizator. In

describing the Totalizator, Haight (then functioning both in Digitronics and in Westbury Electronic) said that while it was believed that this first electronic totalizator would obsolete existing electromechanical machines, "* * * there is virtually nothing in our device which has not already been incorporated in other machines which we have installed for other purposes in such companies as * * *" — and he named a railway and three large industrial companies. His letter continued that, as applied in race tracks, the electronic Totalizator did represent a new departure, and hence it seemed a logical service in advancing the art to provide, if possible, an insurance policy that would cover race track owners against loss.

The prototype had, of course, been demonstrated while it was at Digitronics, and had been used in the attempts to promote sales to NYRA and to the Italians; it was, after it was moved to Roosevelt Raceway in September 1962, demonstrated there. However, the demonstration of the First Tote, which did take place on March 7, 1963, was a spectacular success.

The patent application was prepared starting in January 1963 and it was completed and filed by March 28, 1963. The draftsman of the application was Camil P. Spiecens. He made use of the logic diagrams and of interviews with the various people

concerned in the construction of the First Tote to get the material for the application itself and for the figures used in it; the application was drafted rapidly because it was anticipated that there might be a sale to the Italian group and it was imperative that the patent application be on file in the United States before any sale was made, for otherwise, there could have been no filing for a patent in Italy.

Mr. Spiecens was not told anything about the prototype, and he did not see it or any materials connected with it. He was not shown the brochure written around the prototype (Exhibit U), and he did not know of it. He blocked out the drawings annexed to the patent application, which became the figures of the patent as issued. They were not prepared from detailed working drawings for the equipment itself, but from plant block diagrams and Mr. Spiecens worked with the engineers to come up with block diagrams for the application. Mr. Spiecens also drafted the response to the first office action. There was no interview with the Examiner before the application was granted. The petition for a certificate to corrections was not prepared by Mr. Spiecens.

Spiecens did not see the February 1960

specification of Digitronics for a Fully Electronic Totalizator, but he did recall that at some time he saw Figure 1 of "Exhibit A" (Ex. 94-A) attached to the "January 31, 1961" agreement, Exhibit AP.

The relation between the prototype and the First Tote remains most uncertain. Mr. Weida did not commence to work on the prototype until after Labor Day in 1960, and, although it had been powered up and tried out earlier, as early as late September 1960, perhaps, it was first "demonstrated" in mid November 1960. Mr. Weida replaced Kielsohn on the prototype job (Job No. 4726), and, as found above, when Mr. Weida took over, the equipment was partly wired, he was given the logical design drawings to write up and check, he got the apparently lengthy logic write-up from Shaw, one of the designers, and he talked to Shaw about it, and — in a word — much of the construction was already done and the logic was in hand. Mr. Weida's job was simply to follow through to get operability: the system was complete as a first go-around.

As it happened, none of the people who had worked on the prototype before Mr. Weida took it over worked on the First Tote. Mr. Weida said that the prototype did not "interrogate" the TIMs, nor electronically signal an "unlatch" for rejection, and that

the prototype had little peripheral equipment. The prototype, he recalled, could not handle regular and daily double betting concurrently. The prototype, Mr. Weida thought, did not have reject signal responsive means, and error detection resulted simply in shutting the operation down until the central control started it up again. The prototype, Mr. Weida said, did not put out a bid signal and it had no false entry or scan test.

It is all but impossible to understand how the prototype could have left so dim and uncertain an image after it. Mr. Weida was able to recall that when he took on the job of finishing the prototype, he got 15 to 20 pages of carbon-copy material respecting the operation of the logic and about 20 logic drawings (Tr. 1247-1249), and that he kept these papers for a year or two but cannot say where they went thereafter. There were at least circuit schematic drawings and structural working drawings of some sort, but Mr. Weida does not recall having seen the Exhibit A (Ex. 94-A) annexed to Exhibit AP. The drawings available to him were in the drafting room files.

Whatever the differences, Mr. Weida agreed that Claim 20 of the patent could be read on a mental reconstruction of the

prototype but for the requirement that it contain a plurality of TIMs. However, the evidence warrants the finding and it is found, that in fact the prototype had been demonstrated with two Hohmann TIMs in service, and the simulators, while not genuinely TIMs, would appear from the point of view of their model or demonstration roles to qualify as valid models of "plurality"; their existence is not otherwise justifiable. Mr. Weida appeared to agree that Claim 21 could likewise be read on the prototype, with the same limitation presumably.

The great difficulty was that the drawings for the prototype had completely disappeared, except for one irrelevant drawing, and disappeared without any satisfactory and reasonable explanation of their disappearance. A number of drawings related to Job No. 4726 are listed in Exhibit R but the evidence was that they were missing from the drawer in which they would have been stored. They were uniquely missing; the absence of the drawings reflected a discontinuity in the files.

When the prototype was transferred to Roosevelt Raceway, a set of the drawings went with it, and perhaps the originals, although that is not at all clear; they were not produced from that source, and perhaps they were not available from that source.

The prototype itself remained in storage at Roosevelt Raceway, but it appears to be more or less agreed that the task of trying to determine from it at this date the circuitry and capabilities of the device would be enormous because of the multiplicity of components and the quantity of circuit wiring in any such device.

The continuity of conception evinced in the succession of the May 11, 1959, presentation (Ex.F), the November 1959 outline of the planned prototype (Ex. 94A), and the February 1960 specification for the fully electronic totalizator (Ex.94B); the complete change in personnel assigned to the completion of the prototype at Labor Day 1960; the disappearance of all drawings and of all material relating to the logic of the prototype as the prototype and its logic existed in incompleteness at Labor Day 1960; the unexecuted modification of the Digitronics-Westbury contract of January 31, 1961, which would have eliminated the "sale" and "delivery" language as applied to the prototype and preserved it as to the First Tote; the continuity of conception evinced from the May 11, 1959, presentation to the February 1960 specification, and found in persistence in the Italian presentation of 1961 (Ex. CX), the brochure of 1962 (Ex. U), and the patent itself (Ex. 1); the

patent solicitor's ignorance of the existence of the prototype, of the brochure (Ex. U), or of the early logic writeup of Shaw; Mr. Weida's assent to the idea that, but for the "plurality" of TIMs point, Claims 20 and 21 could be read on the prototype; these are circumstances that, notwithstanding the unshrinking frankness of Mr. Weida's testimony, preclude a finding that the patent presents a conception of the subject matter of the claims of the patent that is of the patentees' invention.

The named patentees, then, had no role in the preparation of Exhibits AP, 94A and 94B; none of them had a role in evolving the design, logic or choice of components of the Demonstrator or prototype; and only the named patentee Weida had any part in the final preparation of the prototype for start-up and demonstration; the contributions of the named patentee Weida to the prototype were at best corrective of blunders in logic detail or implementation and did not either change the controlling logical schemata of the prototype or the plan of tangible embodiment that his predecessors on the project had developed; plaintiff is solely responsible for the substantively unexplained failure to preserve and produce any block diagrams, circuit diagrams or detailed drawings of the prototype or any exegesis of

its logic; and the patent solicitor who drafted the patent specification, claims and the single response to the first office action had no access to those responsible for Exhibits 94A and 94B and for the design, the logic and the supervision of construction of the prototype, did not see the prototype or any demonstration of its operation, did not learn of Exhibit 94A of November 1959 nor of Exhibit 94B of February 1960 (although the latter was directly related to the First Totalisator which was the subject of the patent application he was drafting), and did not know of the printed and published sales brochure of March 1962, Exhibits U, 120 (although a hoped-for Italian sale occasioned the hurried preparation of the patent application on which he was engaged). The testimony of the named patentee Weida leaves no doubt that Claims 20-22 read on the prototype and that the attempt to distinguish the claims made at the trial as not speaking to a plurality of TIMs (Tr. 1814-1823) is wholly unsubstantial. Denied access to everything except the First Totalisator and to those persons named in the patent as patentees, the draftsman of the patent specification and claims had not the means to and did not disclose to the Patent Office examiner or refer in the patent application to the prototype or the published advertising brochure.

Inevitably, the prototype or demonstrator is prior art of other inventors against the patent in suit. It cannot be said that a curable omission of joint patentees is all that is present; 35 U.S.C. 116, 256 countenances no such procedure. The named patentee Weida cannot be treated as a joint inventor both of the prototype and of whatever, if any, improvement on the prototype may have been represented in the disclosure of the patent in suit and embodied in the First Totalisator. Rival Mfg. Co. v. Dazey Products., W.D. Mo. 1973, 358 F.Supp. 91, 102, 177 USPQ 432, 440. It is no answer to point out the fact that all the Digitronics personnel involved had alike signed agreements entitling Digitronics to claim from them assignments of their patents and patent rights growing out of their work for or related to the business of Digitronics.

The prototype was repeatedly and successfully demonstrated more than a year before the patent application was filed. It was delivered to Roosevelt Raceway in 1962 and has since remained there, and the costs of its manufacture were paid for by Westbury. However, the demonstrator or prototype was not practically operable as a racetrack totalisator; it was a demonstrator only; not a toy, not a model; it was a full

scale demonstrator and it was meant to be used and was used first as a demonstration to Roosevelt Raceway and, later, as a demonstrator for Westbury in its sales efforts; it had been hoped it might be used to get state approval of the full sized totalisator of Exhibit 94B (Exhibit AP, Exhibit B), but that was not accomplished. But neither such "sale" as there was of the prototype (and nothing turns on the inept effort to rewrite the contract, Exhibit AP), nor such use as was made of the prototype as a demonstrator, reached the disabling level that 35 U.S.C. 102 marks as being "in public use or on sale in this country."[8] The sale was not on commercial terms for the ultimate use to which the projected finished product would be devoted, nor was the use, if public, a use of the article of the patent rather than a use of an illustrative but commercially incompetent prototype of the article of the patent, and it was not a use for the purposes to be served by the article of the patent but a use in order to demonstrate the validity of the scheme of the article of the patent. Cf. Cali v. Eastern Airlines, Inc., 2d Cir. 1971, 442 F.2d 65, 70-71, 169 USPQ 753, 756-758; In re Yarn Processing Patent Validity Litigation, 5th Cir. 1974, 498 F.2d 271, 277, 282-285, 183 USPQ 65, 72-75; Jack Winter, Inc. v. Koratron Co. Inc., N.D.Cal. 1974, 375 F.Supp. 1, 37, 181 USPQ 353, 373-374.

The printed and published brochure, Exhibit U, has a two-fold importance. *First,* within Section 102(b) it is beyond question a printed publication in this country; if it discloses an invention, whether that of the patentees or that of Shaw and Kielsohn, that is final: it is either (or both) prior art against the patent (Section 102(a)), or a disabling printed publication (Section 102(b)). *Second,* it relates, along with Exhibit 94B, to the sale of the First Totalisator, and, by its relation to the prototype, viewed as a reduction to practice of the invention of the patent (although it is rather a reduction to practice of the invention of Shaw and Kielsohn, the predecessors of Weida, et al.), relates to the idea that there can be a sale of future goods that is disabling under Section 102(b) if the article is one that in ordinary trade would be sold as future goods to be built and if, at the time of contracting, it is sufficiently defined, provided, at minimum, it has been reduced to practice in some reliable, complete manifestation. Can it fairly be said that the First Totalisator was on sale a year before the filing of the patent application drawn from the First Totalisator as it was completed and before it was publicly demonstrated? Cf. Jack Winter, Inc. v.

Koratron Co., Inc., supra, 375 F.Supp. at 37, 183 USPQ at 72-75; Kalvar Corp. v. Xidex Corp., N.D.Cal. 1973, 384 F.Supp. 1126, 1130-1138, 182 USPQ 533, 535-542; Philco Corp. v. Admiral Corp., D.Del. 1961, 199 F.Supp. 797, 814-818, 131 USPQ 413. Contrast Burke Electric Co. v. Independent Pneumatic Tool Co., 2d Cir. 1916, 232 Fed. 145, 146-147, 234 Fed. 93. Robbins Co. v. Lawrence Mfg. Co. 9th Cir. 1973, 482 F.2d 426, 431-433, 178 USPQ 577, 580-581 may be taken to suggest that in the case of a sale of future goods to be built to specification, where there is no fully operative device in existence, a finding that the article of the patent had been put on public sale could rarely be warranted. The history of the "sale" of the First Totalisator does not reach any of the uncertain benchmarks that the cases seem to limn. Roosevelt Raceway's shilly-shallying, the cutback in scale, the grouping for cost savings and for a ceiling on costs that kept running out of hand, these fluid factors combine to preclude a finding that there was an August 1961 contract to sell the First Totalisator as an article complete in design, specification and detailed drawings and adequately exemplified as a feasible device by the prototype. Without such a finding, it cannot be held that there was a disabling contract to sell within the meaning of 35 U.S.C. 102(b).

II

Untangling the patent from the bramble of unfamiliar terminology is not very easy, but the 25 day trial illuminated the darker corners and, it is believed, made possible a reliably simple explanation of the teaching of the patent against the background of the prior art. Analysis leads inevitably to the conclusion that the claims of the patent now in suit, claims 20 through 27, are not valid claims.

To start at the beginning, data processing, whether mechanical, electromechanical, electronic, or solid state electronic, takes advantage of the facts that numbers can be reduced from decimal or whatever other number base is used to binary notation in which the only digits are zero and 1, and that the steps or stages of mathematical reasoning can be starkly expressed in algebraic form, not so far removed as might at first seem from Aristotle's use of letters in, for example, the Prior and the Posterior Analytics. As will be seen, the patent refers to a Boolean equations (Columns 11-15); the reference is to George Boole and to his epochal alegebra of classes. In his book, An Investigation of the Laws of Thought, on which are founded the mathematical Theories of Logic and Probabilities, he says:

> "Hence, instead of determining the measure of formal agreement of the symbols of Logic with those of Number generally, it is more immediately suggested to us to compare them with the symbols of quantitiy <u>admitting only of the values</u> 0 <u>and</u> 1. Let us conceive,

> then, of an Alegebra in which the symbols $\underline{x}$, $\underline{y}$, $\underline{z}$, &c. admit indifferently of the values of 0 and 1, and of these values alone. The laws, the axioms, and the processes, of such an Algebra will be identical in their whole extent with the laws, the axioms, and the processes of an Alegebra of Logic. difference of interpretation will alone divide the." (Boole, The Laws of Thought, Dover Reprint of the 1854 edition, pages 37-38.)

According to tradition (see Exhibit K) it was in 1938 that C.E. Shannon demonstrated that a Boolean algebra could be adapted to the presentation of data processing circuitry, and could be used in evolving and simplyfying data processing circuitry. The principles of the Boolean algebra involved turn on the limitation of values to 0 and 1, the recognition that the Boolean algebra involved is essentially an algebra of classes, and the fact that a system limited to the values 0 and 1 could nevertheless also be used for limitless enumeration as the digits of a binary (or base 2) system of numbers. In Boolean algebra as a logical system the rules of operation take an unusual form (as explained in Exhibit K, Chapter 2 of Richards, Arithmetical Operations in Digital Computers). The familiar plus sign has the meaning of "or"; the multiplication sign (indicated by the x, the dot, or simply by writing two letters close together without punctuation or separation) has the meaning of "and"; with the logical reading that 0 plus 0 equals 0, as always; 0 plus 1 equal 1, as always;

and 1 plus 1 equals 1, because, in the logic of this Boolean algebra, the expression means that 1 or 1 equals 1, or, to put it another way, it states that if there is a class of 2 members either or both having a certain defining characteristic, then a statement that one or the other or both members of the class have the defining characteristic is true, otherwise it is not. Mr. Weida (one of the patentees) in Exhibit 149 put the ideas of this arithmetic in essentially truth table form; using instead of 1 and 0, or "true" and "false," 1 volt and 5 volts where 5 volts represented the critical voltage required in the circuit, he essentially was using truth table analysis of what is meant by disjunction. That is, treating the plus sign as the sign of dijunction, then A plus B equals C would yield the following truth table:

$\underline{A}$	or $\underline{V}$	+ $\underline{B}$	or $\underline{V}$	= $\underline{C}$	or $\underline{V}$
F	O	F	O	F	O
T	5	F	O	T	5
F	O	T	5	T	5
T	5	T	5	T	5

In Figures 2, 3 and 4 of the patent, Exhibit 1 and in the specification, if it is intended to show or state that two input wires are to energize a third wire beyond a certain gating point if either or both of the input wires bears a signal at the critical voltage level but not otherwise, the input wires are shown entering a square labelled "0" (the symbol

for an "or" gate) and one wire is shown emerging from that gate. The circuitry significance is that if either or both input wires are energized to the critical voltage level, then the "or" gate will permit the energization of the efferent wire; it will interdict energization of the emerging wire if, but only if, neither of the input wires is energized to the critical voltage. In the figures of the patent, conspicuously figures 3 and 4, the "or" gates are numbered as well as identified as "or" gates by the letter O. So in figure 3 at the very top towards the center will be seen a square box with the identification 01. It is illustrated with four input wires along which signals could proceed. In the logic of the device that means that if any one or all of the inputs to the "or" gate "01" is energized, it will send an energizing signal to the next component, in this case the step pulse generator. Other "or" gates will be seen in figure 3, conspicuously, "or" gate "03" at the lower left which has five input and one efferent wire, again signifying that if any one or more or all of the input wires carries energy at the critical voltage level then the efferent wire will be energized.

In the Boolean algebra of this circuitry the multiplication sign is identified as "and," with the immediate Boolean algebraic significance that 0 times 0 equals 0, 0 times 1 equals 0, and 1 times 1 equals 1. The multiplication, or "and," function in the Boolean algebra of computers means that if, and only if, all of the inputs are 1 will the output of the "and" gate be 1. Mr Weida illustrated this in exhibit 149, and, again, extended

the form of the truth table to gather in the "and" gate function. Put in true/false truth table form, and in parellel with A times B equal C, the table would be as follows:

A	or	V	X	B	or	V	=	C	or	V
F		0		F		0		F		0
T		5		F		0		F		0
F		0		T		5		F		0
T		5		T		5		T		5

Referring to figures 3 and 4 of the patent, Exhibit 1, the "and" gates will be seen to be those which are identified by an "A" followed by a numeral inside a square. In figure 3 at the upper left hand corner is "and" gate 1. It is shown with two input and one efferent signal wire and has the effect that if, and only if, both input wires are energized to the critical voltage will the "and" gate energize the output wire leading to the next gate, which is "or" gate 1, mentioned above. In figure 4 at the extreme left and near the top of the figure will be seen "and" gates A8 and A9, each shown with three input wires and one output wire. The significance in each case is that if, and only if, all three input wires are appropriately energized will the output wire leading to the "or" gate 05 be energized. It will be seen here that "or" gate 05, which receives its input from "and" gates 8 and 9, will energize its output wire if the gate's input is energized from either or both of "and" gates A8 and A9. (It will be noticed that

all the signals shown as entering A8 have a capital A in their identification. This reflects the fact that, as figures 1A and 1B illustrate, the system of the patent has duplicate units identified as A and B.) The sense of the A8, A9, 05 gating is that if either the A or the B side is energized at the required level, or both sides are so energized, the "or" gate 05 will send a signal to "and" gate A10, which in turn, will emit signal SCNI if, and only if, it receives signals from all of "or" gate 05, "flip-flop" CONA, and "or" gate 017. Only if neither the A side nor the B side signals are sufficient to energize their respective "and" gates A8 and A9 will "or" gate 05 fail to send on a signal to "and" gate A10.

The logic of the Boolean algebra employed contains the idea of negation with the necessary consequence that the negation of 0 is 1 and the negation of 1 is 0, since they are the only digits or values used in the symbology. The negation of any variable is indicated by putting a bar over it or using a prime mark to the right of the letter or letters identifying the variable. In the specification of the patent the prime mark is used. The logical principle of the Boolean algebra that 1 + 0 = 1 requires the conclusion that, using A as the variable, A plus A' equals 1. Similarly, A times A' equals 0, since, as above, 1 X 0 = 0. And, finally, A" = A. That is, a negation of a negation is the equivalent of an assertion, and this will be true whether A is 0 or 1, since the negation of 0 is 1 and the double negation of 0 is 0 and the negation of 1 is 0 and the double negation of 1 is 1. The

negation function is employed in computer algebra and is illustrated in the circuitry of the patent by a square box in which there is a letter I, meaning inverter, followed by a number. The effect of the inverter is that if the input is a critically, positive voltage, then the output negates the functional significance of that critical input voltage. More generally if the input is 1 then, for circuit purposes, the output is 0, and vice versa. The negation function is illustrated in figure 3 of the patent at the upper left as square boxes 11 and 12.

The specification repeatedly refers to flip-flops, best seen at the right side of figure 3; the five large squares each with a "0" near the top and a "1" near the bottom, and with identifying letters "TFBF," etc., inscribed in the middle of the box, are flip-flops. In the middle lower left of figure 3 there is a box that has inside it the identification "ERAF"; it is a flip-flop, but, apparently through error, the 1 was not inscribed in it.

The flip-flop function is explained at pages 47-49 of Exhibit K. Very broadly it is a "bistable" function which has the capacity to store a 0 or a 1 until it receives a new pulse (of appropriate voltage) which changes its state to the opposite. That is, if it is in 0 stable state, the impulse will change it to 1, and if it is in the stable state 1, the impulse will change it to the stable state 0.

Finally, in the figures of the patent, Exhibit 1, there appear a number of "delay" units symbolized by a square box in which there is a letter D together with an

identifying number. One such is shown in figure 3, at the bottom center, as D4. Two other delay units will be seen higher up in figure 3 just below the mid-line; others will be seen at the right of the figure.

The specification and figures of the patent are largely written in the language and using the symbols exhibited and discussed in Exhibits K, M, N and L, all excerpts from Richards, Arithmetic Operations in Digital Computers, which is referred to in the patent at column 12, lines 3 to 5, lines 10 through 21 and lines 32 through 36; at column 13, lines 53 to 56; and at column 15, lines 26 to 31 and lines 58 through 60. It will be seen particularly in Exhibit K that Richards, a 1955 publication, conducts much of the discussion in terms of the logical diagrams without reference to the particular means of performing the logical function, and that he explains their use with either solid state diodes, or vacuum tubes, or electromechanical relays.

Two other preliminary matters are needed for a good reading of the patent. The patent repeatedly refers to memory, and memory is manifestly a basic part of data computing and solid state electronic data processing. The individual building block of the memory or core memory is a tiny toroid or anulus which can be polarized, in the sense of establishing the direction around the periphery of its magnectic field, either in a clockwise or counterclockwise direction; it can maintain the direction of polarity of its magnetic state until the polarity is reversed by a fresh impress of current upon it. The

toroids used in the memories here involved are apparently 1/16 inch or less in outside diameter and can each store only one "bit" or information datum, since they have only two states, counterclockwise and clockwise magnetic fields. AS the system is aimed at the use of a binary logic, inevitably the two states are read as one and zero. A memory core to be useful, then, must have a very large number of toroids in it, and, since each one of them has only the capacity to represent either a 1 or 0 that is either a part of a binary number or part of some numerically encoded information that is in storage, or is being brought out of or restored to storage, it must be locateable and accessible. In the language of the patent and the art, it must have an address. Physically, the memory may be a cube or other rectangular solid in which the toroids are stacked like poker chips in row and column. A memory might measure 64x64x25 toroids, each at a fixed and permanent location in the memory, and each individually accessible to wire conveyed impulses that impress on it a clockwise or counterclockwise magnetic field, and, therefore, a 1 or 0 significance. To determine, and by determining to "read out," its 1 or 0 meaning, a current is applied to it which will alter its polarity of manetization (and in so doing emit an output signal) if it is in one state but not if it is in the other state, thus extracting its "bit" of information from it. For whatever purpose, that bit has been retrieved. See Exhibits 13 and BN, BO and BP. Since every such bit will have been "read out" from and restored to an identifiable location on a specific magnetic toroid in the same or altered state,

a change of its state between pre-readout and post-restoration, from 1 to 0 or 0 to 1, reflects the alteration of the binary number-place which it represents; that is, it reflects an addition or subtraction. For example, if a toroid represented the first number-place at the right end of a binary number, and had been 0, and upon restoration, it is 1, then it will be plain that one wager (or whatever) has been added to the "word" in the memory of which that toroid's bit of information formed a part. The same thing will be true whether the position of the toroid is at the extreme right number-place or any of the other number-places along the row of a binary number. It will reflect either a change in the quantity represented by that number-place or a retention of it, for not every addition to a binary number changes the state of every number-place in the number. The number 101 is binary notation, when it has one added to it, becomes 110, the number-plave at the left remaining unchanged. In the memory illustrated in Exhibit 13, the "words" stored are represented by stacks of 25 toroids, a "long" enough word to accomodate a very large number together with keying data necessary to the effective handling and processing of the number.

Sections of the memory can also store, coded in binary numerical form, instructions to govern the steps in the functioning of the device, so that no human operator is needed to take the results of one step in the process and set in motion the next operation, as is required with calculators. The stored instructions are drawn from the memory and entrained with the data

being processed so that they can perform their roles as active signals operating on the data through the circuitry provided in the device.

As Exhibit 13 illustrates, each magnetic toroid is reached for its bit of information by being found at the intersection of two wires which traverse its open center. Advantage is taken of the fact that each magnetic core toroid can be magnetized to saturation so that added current in the same sense will not change its magnetic polarization, and that if it has one polarity, it will take a critical amount of current to switch its polarity reading from 1 to 0 or from 0 to 1. Since it takes an intersection of two wires to locate the toroid in the memory, less than the critical current is applied on each of the "select" wires that range the memory from two directions to intersect at the toroid. Since neither wire has the critical amount of current on it, they will not change the state of any of the toroids they traverse until they meet at the toroid of choice; there the union of the two less than critical currents, summing to a more than critical current, will change the polarity of the toroid if it is opposite to that of the select currents or leave it unchanged if it is of the same polarity. The change in polarity is read out on a sense wire as a wave form pulse, leaving the core toroid bereft, but receptive to restoration of the same or a different magnetic polarity after the operation is complete. The read-out of a pulse or of no pulse is, of course, equally communicative of the toroid's stored bit of information.

Such a read-out is "destructive." To restore the "word" to its "address" in the same or altered form requires the regeneration of the location by fresh signals.

A second aspect of the reading of the patent involves the interpretation of the lines drawn on the figures and the progess of signals from one to another place. Signals, that is, data communicating signals which will communicate 1 or 0 from one point to another can, evidently, be a sequence of timed electronic events speeding along a single wire, or the signals can proceed along parallel wires, and, plainly, the latter is, in a subworld of blindingly fast travel, much quicker, since all the data are communicated in the lapse of time required for communicating a single impulse. Hence, while most if not all of the wired connections in the figures of the patent are shown as single wires, that is schematic. In many cases the single wire is really a bundle of distinct strands each capable of transferring one bit simultaneously with the transfer of other bits on other strands of the same "wire."

As stated above, the patent is not easy to read and the reading is complicated by the fact that the specification is written around the daily double capability of the system and its use substantially throughout of duplicate components and duplicate processing of the critical signals, neither of which aspects of the patent is involved in claims 20 through 27, the only claims here involved. Plaintiff introduced the case by having the first named patentee, Robert L. Weida, testifying as an expert,

explain the system from the patent's summary, and then take a wagering transaction through the system. That involved something more and different from what he did later in applying claims 20 to 27 to the figures of the patent to show the significance of the means specified in each of the claims and how they functioned. These approaches require a reading of the specification of the patent, and the reading becomes important in part because of plaintiff's reliance on so much of Section 112 of the Patent Law as provides that

> "An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."

In an effort to make the specification more readable, sketches of the figures of the patent (Annex B, C and D) have been prepared which, so far as is possible, are restricted to the matter necessary to the reading of the claims in issue and can yet indicate the working of the whole system as a "simplex" rather than a "duplex" system, eliminating daily-double circuitry where possible.

Annexes B through D present versions of the Figures of the patent (1A, 1B, 2, 3, and 4) from which have been eliminated

the "B" elements, those elements limited in their use to the dual aspect of the system or to daily double betting, and elements not germane to the claims, and Annex A presents a versions of a block diagram showing, in the main, the components germane to the claims in a form that seeks to stay close in usage to the Figures of the patent.

III

The patent is entitled a patent on a "Data Processing System" and each of the claims in suit is a claim upon a "system comprising" a plurality of TIMs or a TIM followed by a combination of particular means. The specification then continues - and so much of it is paraphrased as relates to the claims and is needed to explain the role of the matter covered by the claims:

The invention pertains to data processing systems and more particularly to systems for processing data received from TIMs, one of the commonest of which is a parimutuel system for servicing wagers on sporting events. Existing systems are slow operating, of only average reliability, are dependent on must human assistance and have limited versatility. Such systems, however, can neither tolerate down time during the wagering nor errors in processing wagers. A general object of one aspect of the invention relates to down time and reliability.

Downtime and reliability aspect: A data processor is provided for processing transactions having a plurality of pairs of units, each unit duplicating the function of the other, but one being the master

and the other the slave unit. Disregarding the pairing aspect, checking means are included in each separate unit for checking for erroneous transaction signals so as to transmit an erroneous-transaction indicating signal to the master selecting means. The invention includes various checking means for detecting erroneous transaction signals, for deactivating the data processor when the checking means in both paired units detect erroneous transaction signals in them, and for rendering ineffective the unit which detected erroneous transaction signals. A general object of another aspect of the invention is to provide a high speed scanning means for interrogating a plurality of relatively slow operating TIMs for transactions.

High speed scanning aspect: Scanning means are provided for sequentially and peroidically selecting each TIM for interrogation. Interrogating means transmit an interrogation signal to the selected TIM. If the selected TIM is prepared to make a transaction, it will transmit a selected transaction signal. Means sense for transmission of the selected transaction signal which, if not sensed, causes the scanning means immediately to step to another TIM for interrogation of it.

A feature of this aspect of invention insures that succeeding attempted interrogations by the scanning means of a TIM which has had its transaction either confirmed or rejected do not cause the transmission of redundant selected transaction signals.

Daily-double etc. versatility: An object of another aspect of the invention

is to provide a more versatile system by providing for processing sequential multi-entry transactions such as daily double wagers.

The system includes a plurality of TIMs which accept transactions on entries in a horse race (for example). The transactions are operated upon by a data processor. The data processor includes common units such as a Console, a Scanner, Buffers 1a to NA (there being one buffer for each horse running in the race), a transaction processor MRA (all seen in Fig. 1-A) and a transaction calculator TCA seen enclosed in dotted lines at the lower left of Figure 1B. The transaction calculator TCA includes a plurality of registers (MEM A), a portion of which are aggregator registers; aggregated transaction updating means (UAA); a computer (COMA); ("Error Unit" ERCA) and an acknowledge unit (AKA).

The system of the patent is described operating in the dual mode with the A side as the master. The left hand units in Figures 1A and 1B have reference characters ending in the letter A. To paraphrase the patent in its simplex mode, using the A side, requires some references to the A master signal means and signals.

A switch in the console C will generate the AMST and AMSTC signals fed respectively to the transaction processor MRA and the transaction calculator TCA, indicating that they are the masters. The AMST signal is fed also to all the interfaces IF1 to IFN (there being an interface for each TIM) so that scanner SCA will control the sequential and periodic interrogation of the TIMs from TIM 1 to TIM N. The

transaction processor MRA will process a transaction, that is, it will check for erroneous transactions and other internally generated errors, and generate storage addresses for the memory positions in the TIM memory (WM, Fig. 1-B), the contents of which are to be updated, and also the addresses of the aggregator registers in the transaction calculator TCA, the contents of which (the aggregated transactions) are to be updated. The transaction information processed from the transaction processor MRA is fed to the transaction calculator TCA. The transaction calculator TCA operates on the processed transaction information to calcualte odds, pools, payoffs and similar information.

All units are connected by signal lines which transfer signals between the units. Signal lines bear the same reference characters as the signals on the lines, and this terminology is used interchangeably. Mention of the signal, the, implies the signal line, and vice versa. Furthermore, some signals are shown in a single line for convenience sake, but they are in fact a plurality of lines in a cable. The lines AADR, WADR, MOA, MIA, SKNA and SKRN are typical examples. Moreover, the lines shown indicate only one polarity of the signal line in some instances a parallel line carries the opposite polarity of the signal, indicated as BID1'(the prime mark being used to represent a negation often indicated by a bar over each letter being negated).

Switches on the console C determines which side (A or B) is master. Console switches also initially clear the system (by dispatching the ICL signal) through momentarily depressing the "initial clear"

switch SIC, and console switches also indicate the entries (horses) upon which no transactions will be allowed ("scratches") by positioning the "non-transaction" switches SKWN which generate the associated non-transaction signals SKRN.

The console also includes a three-position mode switch SFS which, when in the "D" position, indicate the dual mode, when in the "A" position, causes the generation of the FSA signal indicating the simplex mode with "A" the master, and when in the "B" position, generates the FSB signal indicating simplex mode with "B" the master.

The AMST signal fed to the interfaces IF1 ... IFN (and there is an interface for each TIM) sensitizes these units to interrogating signals such as the SCNNA signal from the scanner SCA (see Annex B). The AMST signal fed to the transaction processor MRA insures that storage address signals are fed only from the transaction processor MRA to register MEMA and TIM memory WM (probably "WM" means "Window Memory," that is TIM memory). Similarly, the AMSTC signal fed to the transaction calculator TCA insures that only its data are fed to the output line (OUA).

The ICL signal fed to the transaction processor MRA presents to its initial count of one the scan counter SKA, which is a typical chaim of conventional cascaded binary counters in which each binary counter has an output both from its "1" and "0" sides, (Annex C, extreme right, lower half of page). The output of scan counter SKA is fed as the SKNA signal from transaction processor MRA to the scanner

SCA, which is a typical decoder which decodes the combinations of "1s" and "0s" from scan counter SKA. The SKNA signal is decoded by the scanner SCA and becomes the SCNNA signal which goes only to interface IFN, the interface of TIM N (see Annex B). If TIM N wishes to make a transaction, then one of its transaction keys will have been depressed and IDN signals will be received by the interface IFN, but will have no effect unless and until the scan is at TIM N for interrogation.

When the scan is ready to interrogate TIM N for the wagering transaction, the SCNNA signal passes (via IFN) to TIM N as an SCNN signal, which is fed to the common side of all the transaction-selection switches of TIM N (see Annex B, Annex D). This signal will pass through to the other side of the closed transaction-selection switch and be fed out as a selected-transaction HIN signal to buffer 1A (see Annex B: the 1 in the signal designation HIN and in the buffer designation 1A indicates the horse, or "entry," numbered "1." No matter how many TIMs there are, and the TIMs are thought of as being an indefintely large set, TIM 1, TIM 2, ... TIM n, all wagers on starting horse No. 1 will feed from the N TIMs to buffer 1, all wagers on horse No. 2 will feed to buffer 2, and so on through the N starting horses; the starting gate capacity sets the maximum number of horses that can contest any race.) For example, if the entry is being inserted as a wager on horse 1 (see Exhibits 11, 14 and 15), entry key 1 of the TIM N would have been depressed, causing the associated transaction-selection switch to close and latch, and an HIN signal would feed through

buffer 1A to become the particular entry HIA signal fed to transaction processor MRA (See Annex B). The H1A signal is stored in the entry register 1 HRA in the transaction processor MRA (see Annex C).

At the same time, Control KA (see Annex B, C; KA is in the transaction processor MRA) transmits a test-for-transaction-made TFB signal, generated by flip-flop TFBF (Fig. 3, upper right), to probe the transaction-made unit BMA (Annex C, lower half). (The lettering signifies "TFB" - test for bet signal; "TFBF" - test for bet flip-flop; and "BMA" - bet made unit. The A indicates, again, the A side of the dual system. The F at the end of TFBF is the indicator of a flip-flop, seen best in Fig. 3 at the fight where the large squares, arranged one above the other, are all flip-flops. Similarly, in Annex C, upper half, the bottom row of symbols includes flip-flops ERAF and REJF. In Annex D are seen the flip-flops CONAF and REJAF.) If a transaction has been made, as indicated by the presence of a signal on one (and ideally one only) of the H1A to HNA lines from one of the buffers 1A to NA, a BMD signal is fed back to control KA from BMA to start an error-test routine. If no BMD signal is fed back, control KA generates a STEP signal to scan counter SKA (Annex C, lower half) which steps to the count of n + 1 to initiate the transaction-interrogation of the next TIM in sequence. Note that the H1A signal (of HNA signal, as the case may be) results from the SCNN signal's passing through a latched transaction switch, and, if this switch was not latched, the STEP signal was generated. Therefore, this is the method for stepping over TIMs which are not ready with a transaction.

If, however, a transaction-selection switch is latched, and, therefore, one of the H1A to HNA signals is present, it causes a BMD signal to go to control KA, and, as noted just above, an error-test routine starts. The presence of the BMD signal at an input of "and" unit A2 (Fig. 3, upper right) passes a pulse to the "set to 1" input terminal of flip-flop TFTF ("test-for-two" flip-flop), which generates the TFT signal and simultaneously passes the pulse to the "set to 0" terminal of flip-flop TFBF. The first test of the error-test routine after the test-for-bet-made process step is a two-entry transaction test; that is, a test is made to insure that the signals from entry register 1HRA (Annex C, lower half) indicate that only one entry is stored in it. The error risks are that e.g., TIM N faultily transmitted both H1N and HNN signals (see Ex. 16) simultaneously (i.e., one $2 wager on two horses in the same race), or that through a failure in the buffers LA and NA both wagers in a daily-double transaction are transmitted to the first-race entry register, 1HRA (in transaction processor MRA, Annex C). In such case, the two entry transaction test unit THBA (Annex C, lower half) will reply with a THBI (two horses bet input) signal in response to the TFT (test for two) signal from control unit KA (Fig. 3). If that is the case, control KA, sets the error flip-flop ERAF (annex C, upper half) generating the ERA signal and generates the REJA signal (Annex C, Ex. 16A; the TFT and THBI signals reach "and" gate A7; if both are present, they energize the "or" gate 03, which in turn energizes the flip-flop ERAF, which in turn energizes the "or" gate 04, which in turn energizes the flip-flop REJF

and the delay unit D4, from which the REJA signal emanates.) The REJA signal results in unlatching the latched transaction-selection key in TIM N and the ERA signal will make the "message register" MRA ineffective.

If <u>no</u> such error is detected, a THBI' signal is fed to the "set to 0" input of flip-flop TFTF and to the "set to 1" input of flip-flop TFSF, which generates the TFS signal (test-for-scratch) to test for the selection of an entry upon which no transaction will be accepted, that is, a "scratch." The signal representing the entry stored in the entry register 1HRA (Annex C, lower half) is fed as one of the 1HRN signals to the test for non-allowed transaction unit TFSA (Annex C) and compared with the non-transaction ("scratch") signal SKRN from console C. The TFS signal from control KA probes the TFSA unit (a conventional equality comparator) for equality between the 1HRN and SKRN signals and, if it exists, causes the return of an SKRI signal to control KA, which generates a REJA signal. It also causes the generation of a STEP signal fed to scan counter SKA, for stepping the scan to the next TIM.

If <u>no</u> non-allowed transaction is detected, the next error processing step is performed. An SKRI' signal is fed to one input of "and" unit A4 (Fig. 3), the output of which is fed to the "set to 0" input of flip-flop TFSF and the "set to 1" input to flip-flop RSCF which generates the RSCNA' signal; this starts the false entry test which insures that the signal on one of the lines H1A to HNA truly resulted from the depressing of an entry key. The signal RSCNA' (meaning that the entry is real, not false) is fed from the

transaction processor MRA to all the interfaces (see Annex D). [The specification clearly, and twice, says that signal RSCNA' (the negation or inversion of RSCNA) is fed from MRA to IF1 to IFN. However, Figure 3 shows the "1" output of RSCF as RSCNA and the "0" output as RSCNA', and Figure 1A as corrected pursuant to correction request allowed October 27, 1965 (Ex. 2, p. 105) shows the signals from MRA and MRB to IF1 and IFN corrected from the negative to the positive signals RSCNA and RSCNB. Figure 4, however, shows the negation signal ("no false bet") reaching the interfaces IF1 to IFN (at A8 and A9) to generate, with SCNA and the "A" master signal, via "or" gate 05 and "and" gate A10 the SCNN signal to TIM N. The inference is that the drawing Fig. 1A should not have been corrected. The text, reading it as saying RSCNA', must be taken to mean that RSCF generates RSCNA' <u>later</u>, from the input to its "0" side, from possibly, CONF via "or" unit 02.] However, since the scan is at TIM N (the SCNNA signal), it passes through the interface IFN, where is terminates the generation of the SCNN signal (see Annex D). It will be recalled that the SCNN signal was the interrogating signal was which passed through the latched transaction-selection switch causing transmission of signals through buffers 1A to NA to indicate which horse ("entry") a transaction was being made upon. Therefore, none of the lines H1A to HNA should carry a signal when the SCNN signal is absent. After a delay [at D1, Fig.3] to permit the passage of signals through the loop including TIM N, the RSCNA signal (meaning a false bet indication is present in signal form) is fed to the transaction-made unit BMA (Annex C lower half). At this time, if <u>no</u> signals are generated on the

lines H1A to HNA, a BMD signal is not generated. If, however, the BMD signal, indicating one of the H1A to HNA signals must be present, is generated, control KA - since this is an error - will receive this signal, which causes the setting of the error flip-flop ERAF and the generation of the ERA and REJA signals in the usual way (See Annex C, upper half of page, at "and" unit A6, indicated in dotted lines).

[Note that the BMD signal just described as occasioning the ERA signal is the BMD signal referred to above as being produced when the TFB signal probed unit BMA. That BMD is fed, in control KA, to "and" unit A2 and the output of unit A2 initiates the set of tests of the BMD signal itself for errors.]

When the transaction processor MRA completes a test routine, it generates a signal indicating this fact. For example, after tests are made for "test for bet made," for "test for two-entry transaction" and for "test for non-allowed transaction," concurrent with the "test for a false-entry transaction," the "test-finished" signal TFA is generated by control KA (Fig. 3, Fig. 2, line from KA to SYNA; in Fig. 3 at bottom right the PROA signal to A5 of KA is generated by the coincidence of TFA and TFB signals in SYNA in dual operation).

If an error occurs in the transaction processor MRA, it will be rendered ineffective, it will not generate succeeding test or step-finished signals, but, since it generates an error signal, this signal replaces the test-finished signal (TFA, supra). For example, if transaction processor MRA detected an error, it would

"shut down" and generate the ERA signal, as above. The ERA signal would then replace the TFA signal, the test finished signal, generated by control KA.

After all these error tests have been completed, a GERF flip-flop is set (Fig. 3, lower right). In particular, the coincidence of the BMD' signal (indicating that there has been no false entry) and the RSCNA signal from the "1" out of flip-flop RSCF, delayed [at D1[, as inputs to "and" unit A5 set the GERF flip-flop to "1"; the "1" output of the flip-flop GERF (passing via "and" unit A41 and not via "and" unit A40 since the daily double is not involved) becomes the GERA signal (Fig.3).

The GERA signal "strobes" the storage address generator SAGA (Annex C, lower half, dotted line). The storage address generator SAGA is a plurality of "and" units each having one of its inputs connected to the GERA signal line and other inputs connected to various combinations of the 1HR1 to 1HRN and DKN signal lines from decoder DEC (Annex C, lower half).

The storage address register SAGA, in response to the GERA signal, transmits tow groups of signals. The first group AADRA1 to AADRAM is assocaited with entry transactions; the second group, AADRAM+1 to AADRAN, is associated with the TIMs. These signals are grouped into a cable generalized as an AADRA signal (Annex C, lower half).

The control KA generates the "send address" signals SADD (Fig.2,3). The SADD signal is received by the aggregator address transmitter AATA and TIM address

transmitter WATA (Fig. 2). The first and second groups of the storage address signals AADRA pass through the aggregator address transmitter AATA to become the aggregator AADR signals; likewise, the second group of AADRA signals passes through the TIM address transmitter WATA to become the memory position address WADR signals (Fig.2). Since single wagers, and not daily double wagers, are here considered, only the 1HR1 to 1HRN signals and the DKN signals (from the entry register 1HRA and the decoder DEC) will be included in the AADRA signals. In the simplex mode, with transaction calculator TCA operating, the AADR signal (from the aggregator address transmitter AATA) is fed to the registers MEMA. Registers MEMA include a multiplane magnetic core matrix which is divided into rows and columns wherein the core in each plane is the same row and column provides a bit storage for a multibit binary number. A group of the registers (aggregator registers) is reserved for aggregating transactions. Other registers are reserved for storing operation and result information of the computer COMA. Included with the registers are typical row and column "selectors" as well as "read" and "write" amplifiers. Each row of matrix associated with the aggregator registers may be assigned to a different entry (i.e., horse), and each column, to a different TIM (see Col. 13, ll 1-14). The addressing circuitry in register MEMA receives the aggregator addresss signals AADR to select the indicated aggregator register. The contents of that selected aggregator address are "read" out, re-circulated, and "written" back into the same selected aggregator register to update the number of wagering transactions. In particular -

for example - the AADR signals when received by the aggregator registers of registers MEMA select the column associated with the TIM and the row associated with the particular entry (i.e., horse) upon which a wager is being made. The signals representing the accumulated number of transactions in that aggregator register are "read" out via the MOA (i.e., memory output) signal lines to the updated by one, and are then fed back via the MIA (i.e., memory input) lines to the original register in registers MEMA. At this time, registers MEMA feed an acknowledgment signal, ACKA, via amplifier AKA, to the control KA, indicating that the transaction has been recorded.

As what has just been related implies, the AADR signal lines are a plurality of lines, divided into two groups. The first group is made up of lines associated with the outputs indicative of wagers made on particular entries (horses), and the lines are coupled respectively to rows in the registers MEMA. The second group is made up of a plurality of lines associated with the TIMs being processed. Under control of a "read" signal the "bits" of the number will be read out of the selected aggregated register as signals on the sense windings connected to the MOA signal lines, passed through a means for updating (e.g., updater UAA) and returned to the same selected aggregator register under control of a "write" signal (such recirculation type magnetic matrices are well known.) (Col. 13, ll.14-22, 27-33.)

The ACKA signal, fed from registers MEMA via amplifier AKA, passes through "or" unit 045 in the control KA (Annex C, upper half) to set the CONF flip-flop to

the "1" state. The "1" output of the CONF flip-flop passes through "or" unit 02 to the "set to 0" input of the RSCF flip-flop, which, again generates the RSCNA' signal, which is fed to the interface IFN to regenerate the SCNN signal (see Annex D). Although the SCNN signal causes an entry to be accepted by entry register 1HRA as described above pp. 92-93, since this is the same entry as before, it makes no difference. The "1" output of the CONF flip-flop also passes through the delay unit D3 to become the CONA signal. The CONA signal is fed to interface IFN, and there, via "and" unit A90, "or" unit 090 and "and" unit A61, to the "set to 1" input of the CONAF flip-flop (Annex D). The CON signal is then taken directly from the "1" output of the CONA flip-flop in interface IFN, as shown in Annex D. (The "and" unit A80 and delay unit D7 relate to daily double betting; they do not funcion regular betting.) The CON signal is fed to the TIM under scan, TIM N, causing the unlatching of the depressed switch and the issuing of the ticket receipt.

The CONA signal also passes through "or" unit 01, (Annex C, upper half) to trigger the step pulse generator STP (which is a conventional delay multivibrator) to generate the STEP signal which, accordingly, occurs after the CONA signal. Therefore, the scan counter SKA is incremented by one so that the next TIM may be interrogated. When the scan steps off TIM N, the BIDN signal terminates, causing the generation of the BIDN' signal which is connected to the "set to 0" inputs of the flip-flops CONAF and REJAF (Annex D).

The step signal STEP clears the entry register 1HRA (Annex C, lower half) as

well as setting the TFBF flip-flop to its "1" state, and the three flip-flops CONF, and REJF, and GERF to their "0" states (Annex C, upper half and Fig. 3).

While the entry transaction is being aggregated (see discussion of MEMA registers, pp. 101-102 above) the specific TIM transaction is also aggregated. In particular, the WADR signal is fed to TIM memory WM. The TIM memory WM is a multiplane magnetic core matrix and assocaited units similar to the registers MEMA, except that its matrix may be considered as having a single row. Of course, it can have many rows, each associated with different entries. The specific addressed memory position in the TIM memory WM is selected in the manner described above for the registers MEMA; the contents of that addressed memory position are "read" out on the WO signal lines and fed via the updater UAW and the WI signal lines back to the same addressed memory position in the TIM memory WM. In this way, a central check is maintained on the number of transactions made at each TIM.

The transaction processor MRA continues in this manner to interrogate sequentially each TIM and to process any wagering transactions that are made. Finally, the scan counter SKA reaches a count that is one greater than the number of TIMs. Therefore, no TIM is interrogated on this step. Instead, the reliability of the buffers 1A to NA is tested for short circuit conditions which would effectively prevent transactions on certain entries during certain periods of time. For example, if an element in buffer NA associated with the line HNN is short-circuited, and the entry number N key of TIM N is depressed while the scanner SCA is pointing to another of the TIMs, then

that other TIM will be unable to complete a transaction on entry N.

The test is performed by transmitting the CHKA signal, derived from the SCNZA signal generated by scanner SCA, to each of the buffers, NA. For simplicity,

CHKA = SCNZA.

The buffers 1A to NA should transmit a simulated transaction on each entry: that is, signals should be present in all of the lines H1A to HNA. Those lines are all fed to the end-scan test ESTA (Fig.2) and a multicoincidence is tested for by the SCNZA signal. If the multicoincidence is not obtained, an $\overline{ESR}$ signal is fed to the control KA (Annex C, upper half, dotted line to 03), causing the generation of the ERA error signal (Annex C). That signal is derived from the flip-flop ERAF at its "1" output, as seen in Annex C.

During all the time until the race commences, the computer COMA periodically performs calculations on the aggregated transactions in order to establish interim accounting results such as odds (Annex B, dotted lines). The computer has access to the aggregator registers which supply the "operands." Error checking is performed during these calculations. If an error is detected by the transaction calculator TCA (Annex B), it generates an error signal. The transaction calculator will become ineffective and cause error unit ERCA to generate a CERA signal. The disposition of the CERA signal relates to dual operation and is not involved in simplex operation. If there is no calculator error, then when an output is desired,

the transaction calculator TCA transmits the result information to the output units, OU (Fig.1-B).

Returning to the cases of detected error: the error flip-flop ERAF (Fig.3) is set to "1" if there is any one of the following signals (for the signal to ERAF's "1" input is derived from "or" gate 03): (a) if there is a false-entry error indicated by the coincidence of the RSCNA and BMD signals at inputs of "and" unit A6; (b) if there is a two-entry error indicated by the coincidence of the TFT and THBI signals at inputs of the "and" unit A7 (Fig.3); (c) if there is a short circuit in one of the buffers NA, as indicated by the ESR signal from the end-scan test unit ESTA to control KA at "or" knit 03 (Fig.2, top, Fig.3, lower left); (d) if there is an inequality error indication, the ERD signal, from inequality tester DU1 (Fig.1A, bottom) - not applicable to simplex operation, or (e) if there is an $\overline{FSB}$ signal which is received by transaction precision $\overline{MRA}$ at control KA from console C, indicating that only the B side is operative - not applicable where the system is operating simplex. The outputs of "and" units A6 and A7 and the FSB, ESR and ERD signals feed inputs of "or" unit 03, the output of which is connected to the "set to 1" input of error flip-flop ERAF. The setting to "1" at any time of the error flip-flop ERAF (which occurs if any one or more of the five signals is present) causes the transaction processor MRA to become ineffective, that is, to drop out. The ERA signal is sent from control KA to console C, which will terminate the generation of the AMST signal.

The ERA signal, which is the "0" output of the ERAF flip-flop, is fed to an input of "and" unit A41 to prevent the generation of GERA signal so that no storage address will be generated by the storage address generator SAGA. [Quaere: A41 is an "and" gate, and the presence at it of a signal seems unlikely to inhibit output. See e.g., Col. 7, line 6 where the presence of $\overline{DD1}$ (also a negation or inversion signal) at "and" gate A41 causes the "1" output of GERF to become the GERA signal. Is the sentence properly, "The "0" output of the ERAF flip-flop ERA' is not fed to an input of "and" unit A41 to prevent the generation of a GERA signal etc."? The signal under discussion is $\overline{ERA}$ which cannot coexist with ERA'.] The ERA signal, however, will pass through "or" unit 04 to the "set to 1" input of the REJF flip-flop to initiate a reject routine.

The REJA signal is related to the REJF flip-flop. That flip-flop is set to "1" whenever the non-allowed transaction signal SKRI or the error signal ERA is generated (Annex C). The ERA signal and the SKRI signal are fed via "or" unit 04 to the "set to 1" input of the REJF flip-flop. The "1" output of flip-flop REJF is fed via "or" unit 02 to the "set to 0" input of the SSCF flip-flop causing the generation of the RSCN' signal, which is fed to "and" unit A8 in interface IFN (Annex D). This signal will pass via "and" unit A8 and "or" unit 05 to become one input of "and" unit A62. The "1" output of REJF flip-flop also passes through delay unit D4 to become the REJA signal (Annex C, top half) which is also fed to interface IFN. Signal REJA passes via "and" unit A92 and "or" unit 091 (Annex D) to become the second input of "and" unit A62, the

output of which is connected to the "set to 1" input of the REJAF flip-flop, causing the generation of the REJ signal which is fed to TIM N to unlatch the latched switch. The output of "or" unit 091 fed to "or" unit 06 may be ignored since related wholly to daily double wagering.

The STEP signal is generated if there is no error and if no CONA signal has been generated as a result of the valid processing of a wagering transaction resulting in the issuance of a ticket receipt. If no transaction is sensed, or if a non-allowed transaction is sensed, it is necessary to "step" to the next TIM without further processing. The first case (no bet made) is indicated by the presence of the BMD' and TFB signals at inputs of the "and" unit A1, the output of which feeds "or" unit 01 (Annex C, upper left). The second case (wherein a non-allowed transaction is sensed) is indicated by the presence of SKRI signal at a second input of the same "or" unit 01. The output of "or" unit 01, when it transmits a signal in response to a signal received at any one or more of its inputs, will cause step-pulse generator STP (Annex C, top center) to generate a STEP signal in the usual manner, and that signal will function as described above.

Scanning is electronically performed at high speed, whereas the TIMs are electromechanical and comparatively lowspeed. To assure use of the high-speed scanning rates the scanner SCA does not wait until the TIM selection-switches unlatch and the TIM prints out the ticket before stepping, but, instead, it steps immediately after initiating these operations.

Accordingly, the scanner might return to such a TIM before the unlatching is complete. Therefore, if no provision is made for such a case, a new transaction will start. To prevent such an error the system provides that so long as a transaction selection switch is latched, the BIDN and BIDN' signals are generated. As described above, for the scan to step, at least one of the CONAF or REJAF flip-flops must be in the "1" state (Annex D). Therefore, when the SCNNA signal is generated, it passes through "or" unit 05 to one input of "and" unit A10, the other two inputs of which are connected, respectively, to the "0" outputs of the CONAF and REJAF flip-flops. Hence, if <u>either</u> flip-flop is set to "1" (rather than "0"), then "and" unit A10 will not pass an SCNN signal (since the "and" unit A10 requires the coincidence of signals from the 0 outputs of flip-flops CONAF and REJAF with a signal from "or" gate 05 to pass the signal SCNN forward), and accordingly, no interrogating signal is generated. No signals will, then, be on any of the lines H1A to HNA, the "transaction-made" unit BMA, when tested as described above, will <u>not</u> send back a BMD (bet made) signal to control KA, and that control will, in consequence, immediately generate a STEP signal, moving the scan to the next TIM in order. Thus the fast moving scanner can pass the slow-operating TIMs without registering erroneous duplications of the transaction underway at the TIM. When, however, the transaction switch finally unlatches, the BIDN' signal sets the CONAF or REJAF flip-flop (whichever of them was set to "1" because of a 'reject" or "confirm" signal) to the "0" state. The next time the scan reaches the TIM an interrogation will be performed.

TIM N, and other regular betting TIMs, may be of the type which includes a bank of entry keys, each associated with a different entry. Each key when depressed closes a transaction selection switch which latches. Each switch is, effectively, of the single pole, single-throw type, having a moving contact electrically connected to a common-input line, and a fixed contact connected to a selected output line, such as line H1N or HNN. The common input line is the SCNN signal line. Ganged to all these switches is a bid switch which generates BIDN and BIDN' signals as long as any transaction selection switch is latched. Included in the TIM in an electromechanical ticket issuing and printing mechanism which is energized by the confirming CON signal to print and issue a ticket and unlatch any transaction selection switches. There is also an electromechanical means for unlatching the switches upon receipt of a reject REJ signal.

Typical buffers 1A and NA are "or" units which will, therefore, pass a signal to the entry register 1HRA in transaction processor MRA, if any, some or all of the TIMs have a valid wagering transaction on the horse whose buffer it is (or if a simulated transaction (CHKA) is present as part of the end-scantest Col.9, lines 8 and following). That is the verbal translation of the Boolean expression of Column 11, line 70.

As noted above, each scan counter (one for the A side and one for the B side when working in duplex mode) typified by SKA, is a chain of conventional cascaded binary counters wherein each binary counter has an output from both its "1" and "0" sides. That is, the binary counter is made up basically of a set, which may be indefinitely large, of flip-flops, each flip-flop being,

obviously, able to represent either a 1 or a 0, and to represent it until a new impulse changes it from "1" to "0" or from "0" to "1." Each flip-flop, then, represents a number place from the extreme right at the decimal indefinitely leftward. If the counter is to function, it must, when set to "1" and in receipt of a signal to add "1," flip-flop to a "0", and carry its original "1" entry to the next flip-flop to its (notional) left. If each of a series of flip-flops extending leftward turned out to be already at the "1" state, the "carry" would go on from flip-flop to flip-flop until it reached a flip-flop that was set to "0", and there the "carried" "1" would come to rest expressing the binary number "1" followed by a series of zeroes ending with the decimal divider. (See Exhibit L and Exhibit 1, column 11, lines 73, 74, column 12, lines 1 to 7.)

The typical scanner SCA is a decoder, which decodes the combinations of "1"s and "0"s from the scan counter SKA. The role of the scan counter SKA is to identify the TIM under scan at any moment of time by its sequential number; a role of the scanner is to decode the binary number in the flip-flop array of the SKA scan counter. The decoded signal from SKA becomes the scan signal SCNNA which, as explained above, goes to the interface and thence, as the signal SCNN, to the TIM under scan, TIM N; there, via the common side of the transaction-selection switches, it reaches the depressed key for the wager being made, and feeds out of TIM N as the appropriate selected-transaction signal, such, for example, as HIN, to a buffer, such as Buffer 1A. The decoder function of the scanner SCA is illustrated in Exhibit M, Figure 3-3(a); essentially that figure

depicts a bank of "and" gates wherein each "and" gate is designed to gate only one combination of binary bits.

The console C performs miscellaneous central control functions in the main manually actuated. Here the scratch switches are located which enable the controller at the console to communicate the scratches electrically to each window, so that the TIMs at that window can be deactivated in some way with respect to the scratched horses or simply be put in a state of caution with respect to them. This is done by imposing a scratch signal on the appropriate lines of the SKR1 to SKRN signal line cable. In addition the console has the starting switch or "initial clear" switch which generates an ICL signal to clear the control elements and to set the scan counter SKA to a start count. The console also has a three position mode switch SFS with three positions D, A and B indicating setting the system to dual mode operation, or setting the system to the simplex mode with either A as the master or with B as the master.

The "means" relating to the unit marked AKA in Annex B lower half, which generates the ACKA signal, is described, column 13, lines 43-44 (and see column 8, lines 9-21) as satisfying a Boolean equation which states that a signal directing that a new total number of wagers on <u>any</u> one of the horses (increased by "1" from the previous total) be restored to the same address from which it was "read out" in the aggregator registers MEMA will cause an "acknowledge" signal to be dispatched to transaction processor MRA.

All the updating means, such as updater

UAA (Exhibit B, lower half, lower left corner) and updater UAW (Annex B, lower half upper right) are "unit adders," similar to each other and of which many were available in the art of 1963. For example, the binary adder shown in Exhibit N in Figure 4-1 (page 84) with slight modification can serve the purpose. That figure depicts a binary "half-adder" system; and the "modifiaction" is to use the number "1" (binary) as a constant addend, thus making the adder specifically a "unit adder" operating to increment by "1" in each operation.

The computer COMA is described as an internally programmed general purpose computer which can perform the necessary arithmetic operations, such as odds computations on the aggregated transactions to produce result information, such as pay-offs. The computer also generates addresses to select the aggregator registers (in MEMA) in addition to its own registers.

Output units take the form of visual display boards, line printers, magnetic tape units, etc.

The transaction processor MRA includes the elements shown in Figure 2 including the control KA, principal details of which are shown in Figure 3 (both shown on Annex C). The entry register 1HRA can be a plurality of flip-flops like those described above. The left had input of each flip-flop is connected to the STEP signal line seen entering at the right side of the entry register. The right hand input of each flip-flop is connected to one particular transaction signal line, e.g., HNA. The "1" output of each flip-flop is connected to one of the 1HR1 ... 1HRN

signal lines. The "0" output of each flip-flop is connected to one of the 1HR1' ... 1HRN' signal lines. The entry register is in effect a set each member of which is a storage place for a single entry and is, in substance, a short-term memory, that being a function that can be served by flip-flops because of their bi-stable characteristic.

The end scan test unit ESTA is a logical element which tests for the multi-coincidence of the simulated transaction signals on each entry line (supra). The Boolean equation as given says that if the simulated signal for every entry key and the test signal are present, then an ESR signal is in order, which would generate an ERA signal. [The Boolean equation calls for the ESR signal when the coincidence is present, but this seems incompatible with column 9, lines 8 to 18; perhaps the right side of the equation should be ESR'.]

The transaction made unit BMA is again a logical element satisfying a Boolean equation calling for the coincidence in the unit, of (a) a wager on one of the entrants in the race and (b) either the test-for-bet-made signal or the test-for-false entry-signal in order to produce a BMD (bet made) signal. The ounter signal, BMD', is produced by feeding the BMD signal to an inverter.

The "test for non-transaction" unit TFSA is a conventional equality comparator which, when strobed by the TFS signal, will transmit an SKRI signal if an equality exists. Such a comparator could be a logical element satisfying a Boolean equation signifying that if in the unit there coincide a scrath signal from the console on

a particular horse and a signal from the entry register of a wager placed on the scratched horse, and the test-for-scratch signal is also present, then the scratch input signal SKRI is generated and becomes an input to "or" gate 01 in control KA. The SKRI signal is fed to an inverter to generate the SKRI' signal. [The SKRI signal is also fed to "or" gate 04 in the control KA.]

The "two entry transaction" unit THBA can be a conventional" majority logical element" which will transmit a THBI signal when interrogated by a TFT signal if at least two of the 1HR1 ... 1HRN signals are coincidentally present. Alternatively a logical element can be employed that would satisfy a Boolean equation stating that if both the TFT signal and signals indicating simultaneous wagers at the same TIM on two different horses entered in the same race coincide in the THBA unit, then the THBI signal will be generated. The two-horses-bet input signal (THBI) then goes to "and" unit A7 in control KA, where, with the TFT signal, it generates one of the signals which can lead to the generation of the ERA signal. (The Boolean equation at column 14 lines 52-55 is misprinted. It is typed correctly in the file history Exhibit 2, 735). The THBI signal is fed to an inverter to generate the THBI' signal.

The storage address generator SAGA, which, as described above, generates a group of signals AADRA1 ... AADRAM associated with entry (horse) wagering transactions and a second group of signals, AADRAM+1 ... AADRAN, associated with the TIMs, functions, as expressed in the Boolean equations of column 14, lines 65 and following, to

produce the AADRA signals associated with the entry transactions (Annex C, lower half), if the GERA signal and the signal for a wager on a horse are both at the storage address generator together; and it then functions to produce the TIM signal group of AADRA signals if there coincide at the storage address generator the GERA signal and the appropriate DKN signal from the decoder, and, therefore, from the scan counter (See Annex C). The decoder DEC is, as its name implies, a decoder similar to the scanner SCA, which likewise decodes scan counter signals.

The aggregator address transmitter AATA is adapted to transmit the two groups of signals to the next stage, that is, it generates the individual AADR signals, as the Boolean equations indicate, if there is the coincidence of the relevant signal from the storage address generator and the "send address" signal SADD derived in the control KA from the coincidence of the delay GERA signal and the negation of the ERD signal as seen in Annex C, upper half, lower right hand corner. The Boolean equation states that the AADR signals will be generated by the aggregator address transmitter AATA if either or both of the A and the B sides of the dual system are functioning. The TIM address transmitter WATA functions in exactly the same way to produce the WADR signals, as shown in the Boolean equations at column 15, lines 15 and following.

IV

It will be evident from what has already been said that the specification was drawn from the First Tote and reflects its electronic makeup. Nevertheless, the language, except in odd places, does not specify or necessarily imply the use of electronic components, and its insistence throughout on generalized expressions that could apply indifferently to electromechanical, vacuum and gas tube, or solid state circuitry precludes a reading of the specification as limited to and selectively invoking specifically electronic means and, within that classification, solid-state electronic means. However, in column 13 the description of the important registers MEMA and TIM memory WM as "multiplane magnetic core matrix" elements, as well as the description of the computer COMA can be thought of as specifically electronic and impliedly solid state electronic devices, and, as pointed out during the trial, column 10, line 72, specifically indicates the use of electronic scanning of the TIMs.

Nevertheless, the descriptive portion of the specification preceding the claims concludes with the typical expression:

> "While only one embodiment of the invention has been shown and described in detail, it will now be apparent to those skilled in the art that many modifications and variations may be made which do not depart from the appended claims."

35 U.S.C. 112 requires no more of the inventor than that he "shall set forth the best mode contemplated by the inventor of carrying out his invention." It is certainly clear that the language of the specification can supply saving specificity to an otherwise too general claim (United States v. Adams, 1966, 383 U.S. 39, 48-49, 148 USPQ 479, 482-483; Singer Mfg. Co. v. Cramer, 1904, 192 U.S. 265, 284-285), but the claims here in question evince a determined breadth and freedom from limitation which seem to indicate that the position of the applicant for the patent was that, since this device was apparently the first completely or substantially completely electronic totalizator and was also a solid state electronic totalizator, the claims should be drafted in broad language so that the fullest range of equivalents could be claimed. The point in any case turns out not to be very important, since the deficiency in patentability is not remedied even if the claims are regarded as limited very closely to the specific device described in the specification and are considered as claiming a solid state electronic

device rather than (or as an improvement over) an electromechanical or mechanical device.

Before discussing the claims of the patent in issue, the history of the prosecution of the application must be referred to. The application was received in the Patent Office on March 28, 1963 and the filing was followed by a petition for special examination which reached the Patent Office on June 5, 1963. The ground of application was that to file an application in extenso would take up to six months and there was a risk that, if the application as filed were found insufficient in its disclosure to comply with the requirements of Section 112, and it took at least six months to prepare a detailed logical and schematic description for filing as a continuation-in-part, the statutory bar might meanwhile have passed, since "the first system which is the subject of the present application was sold on March 31, 1963."

The first office action on the application was mailed August 15, 1963 and it recites that the application had been taken out of turn for examination in accordance with the applicant's petition "for the purpose of determining adequacy of disclosure." The Examiner then stated that the disclosure

was found adequate to support the claimed subject matter and that the application would not be made special for any other purpose than the making of that determination. It was also stated that the application had not been examined to the extent necessary to discover all minor errors.

The references cited by the Examiner were six United States patents; certain pages from the British patent on Univac; the publication entitled Functional Description of the EDVAC; the Chao publication, The System Organization of MOBIDIC; and the Gass publication, Project Mercury Real-Time Computational and Data Flow System. These are in evidence as Exhibits 3 through 3-I.

All claims were rejected. Claims 1 through 19 and 29 and 30 were rejected as vague and indefinite. The Examiner continued:

> "The claims are * * * vague and indefinite in that they recite, at numerous locations, means for performing a plurality of functions, but fail to recite sufficient structure for performing said functions."

The Examiner then rejected Claims 1 through 5, 9, 10, 14, 15, 17, and 18 as fully met by the Chao (MOBIDIC) publication which incorporated one of the six cited

patents, Terzian No. 3,061,192. Said the Examiner:

> "The reference [Chao] shows a data processing system which includes a plurality of pairs of units which may be programmed to; simultaneously process the same problem on both pairs of units (thus duplicating the computation); check for errors in each unit; and allow the non-erroneous unit to predominate."

None of the claims just referred to is involved in the present suit.

With respect to all of the claims, the Examiner said:

> "Claims 1-33, as understood, are further rejected as unpatentable over the Chao publication in view of Schrimpf [U.S. Patent No. 3,029,414] and the British patent [No. 749,836, pages 84-92 and 271-276]. It would appear that applicants have done no more than to select a plurality of individual features from the prior art such as duplexing of equipment as shown by Chao, sequentially scanning a plurality of peripheral devices as shown by Schrimpf, and various error checking features as shown by the British patent, and have incorporated them into a unitary data processing system. Said system, even though an improved one for the desired use, is not unobvious to one of ordinary skill in the data processing art."

Claim 34, the only remaining claim in the original application was rejected as plainly non-statutory, and apparently it is quite agreed that the rejection was correct, although unimportant.

The applicant's response was received in the Patent Office on December 10, 1963, and it was the sole response except for two essentially supplemental communications received in the Patent Office June 3, 1964, making certain additional corrections in the text of the specification and in the drawings. The response was made up of Amendment "A," which presented very modest amendments in the specification and in claims other than those now in suit, and a "Remarks" section which responded to the action of the Examiner. The Examiner's objection with respect to Claims 1 through 19, 29 and 30 — that the claims were vague and indefinite both in certainty of reference and in reciting at numerous locations "means for performing a plurality of functions" without reciting "sufficient structure for performing said functions" — the applicants answered by quoting so much of Section 112 as provides that "An element in

a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure" and by reciting the requirement that the claims particularly point out and distinctly claim the subject matter which the applicant regards as his invention. The applicants pointed to Claim 1 of the patent application which, as amended, read:

"1. A data processor for processing transaction signals comprising:

(A) a plurality of pairs of units, each unit of each pair performing the same function as the other unit but with one operating as a master unit and the other as a slave unit,

(B) a master selecting means for selecting which unit of each pair of units is a master and which is a slave and for changing the selection upon receipt of an erroneous-transaction indicating signal only from the selected master unit, and

(C) checking means responsive to transaction signals being processed in each unit of a pair of units for checking for erroneous transaction signals an for transmitting an erroneous-transaction indicating signal to said master selecting means so that if the

master unit caused said erroneous-transaction signal, said master selecting means then selects the slave unit to be the master unit."

The applicants then referred (as had the examiner) to the language in element (C) of the claim which refers to "* * * checking means * * * for checking * * * and for transmitting * * *" and then continued the argument in this language:

"In other words, the checking means performs the function A and B wherein the function A and B comprises subfunction A and subfunction B. Clearly, this is 'a means for performing a specified function' and falls within 35 U.S.C. 112. The alternative approach would be to amend the element to read 'checking means * * * for checking * * * and transmitting means responsive to said checking means for transmitting * * * when said checking means detects an * * *' It is believed that such an approach would clutter the claims with unnecessary verbiage and would not *particularly* point out and *distinctly* claim the invention."

There was no further discussion of the Examiner's objection.

The response did not direct the Examiner's attention to any place in the

specification which particularized the structure, material or acts which the means language invoked. Presumably, it would be the whole of the error detection circuitry described, together with the circuitry for determining whether the error was common to both sides of the system, or to one only, and the means for changing master. The patent specification is, however, essentially written in terms of logical functions and not in terms of "structure, material, or acts described," even in the "Description of the Elements of the System" section starting in Column 11. In a word, the specification does not advise a licensee what "means" components or elements he should order from a manufacturer or include in his bill of materials in order to put together the "means" referred to. The response did not meet the Examiner's point, but rather turned it aside with a semantic parry not addressed to whatever substance was in the criticism.

The applicant discussed the Chao article on MOBIDIC strictly in terms of MOBODIC viewed as presenting a duplex or dual system. It may be noted that the discussion portion of the MOBIDIC paper (Exhibit 3-H, pages 106, 107) suggests that the applicants erred in saying that the

MOBIDIC system did not operate simultaneously on the same data, and did not compare the output of the two processors and error detection means. The deeper inadequacy of the applicants' response to the examiner's discussion of the Chao article on MOBIDIC is that it discusses only the duplexing aspect of MOBIDIC and of the somewhat related Terzian patent (No. 3,061,192). None of the claims directly in suit is on the dual or duplexing operation of the device of the patent.

The Examiner's reference to the Schrimpf patent (No. 3,029,414, Exhibit 3A) is answered by saying that the Schrimpf patent merely showed "a single scanning means for scanning a plurality of input-output devices which, when it finds a demand at a particular input-output device, sets the computer into a subroutine which then ties up the computer to store information in the main memory." Schrimpf, it is aruged, was not remotely concerned with the interactions of TIMs and computers, wherein, in addition to scanning, there is direct control of the TIM reaction, that is, whether to issue a ticket or reject the transaction. It is argued, too, that Schrimpf does not prevent duplicate entries of the same transaction (because of the slow operating input device)

and does not remotely suggest handling multi-entry transactions. Certainly it is plain that Schrimpf does not anticipate Weida, but that was not the Examiner's point in citing it. The Examiner instanded Schrimpf's sequential scanning of a plurality of peripheral devices, and so much Schrimpf does, indeed, opulently teach, specifying demand lines that indicate when a particular peripheral device is in condition to receive or transmit information and a responsive scan signal in the form of an operational control signal generated by a traffic control circuit for purposes of initiating a control operation directly related to the demand line from the peripheral device which is then active. In addition Schrimpf specifies a second and separate system of scanning (traffic control circuit identified by the numeral 12) which sequentially scans a separate set of demand lines, the sequence register demand lines. The purpose of the second scanning is to supply a traffic control system for sequencing a plurality of programs, since it is visualized that the peripheral devices may be demanding execution of different programs. Schrimpf does provide error detection means (as seen from Fig. 2B). The indication is that the error signal would be generated if an error occurred in the course

of performing an order called out by any one of the sequence register selection signals.

The response similarly differentiates the British patent, referred to by the Examiner for its display of various error checking features, by observing that under the British patent error detection stops the computer, whereas in the system of the patent error detection requires switching to the second circuit, thus minimizing the possibility of stopping the computer entirely. But again the Examiner's point was not that the British patent anticipated Weida or any of the particular subsystems within Weida on which claims were based, but that the British patent showed various error detection features, which it undeniably does. The British patent refers to duplicating circuits in order to check on arithmetic operations without interrupting computation; it performs the computation simultaneously but independently in separate units, and compares the answers of the two circuits for discrepancies indicative of error through a half-adder called a like-unlike or comparison checker. The British patent also indicates that most of the important system units are duplicated, and that there are eight comparison checkers throughout the computer, so located that every arithmetic or transfer operation is checked by a comparison checker (see Ex. F, pp. 84, 86 second column, 87 second column, and 271 first column).

The applicants' principal argument, of course, was to point out that merely finding features of the claimed invention scattered among different references in the prior art is not significant unless the references "suggest the combination" presented by the applicants' claimed invention; it is argued that the references of the Examiner do not suggest (in Chao's case) the parallel operating and switching concepts claimed by applicants nor does Schrimpf teach the "inventive concepts concerned with the interaction of the input machines and the remainder of the system," nor does Chao suggest adding a scanner and a plurality of ticket issuing machines to his computer system or solving the problems created thereby — the problems dealt with in the applicants' device. But, although it is true that a combination patent is never invalid simply because no one of the elements of the combination is itself separately patentable, it is equally a truism that the fact that the combination cannot be shown to have existed earlier does not establish patentable utility and novelty. What is old always suggests a range of uses that is a function of the essential nature and attributes of the article and method. Its suggestiveness is not

confined to the known instances of past use. The combination must be unobvious. It must do something more than or different from what any linkage of the separate elements would, from their very nature, accomplish. In other words, the combination claim must be not simply unobviously new but, in the language of the Court, must have something approximating a synergistic effect. Anderson's-Black Rock Inc. v. Pavement Salvage Co., Inc., 1969, 396 U.S. 57, 59-61, 163 USPQ 673, 674-675.

The patent prosecution really went no farther. There was no interview, no further submission, other than the corrections referred to above. The patent and all 33 of the claims, with the modest corrections made in some of them, were then allowed. The claims presently involved, Claims 20 through 27 were allowed without amendment, exactly as filed.

No doubt the Patent Office's task of going through applications for patents on elaborated data processing systems is a daunting one; invention is likely to lurk in some special aspect of the system or

device not easy to isolate in the necessary welter of detailed circuitry inevitably presented. But it is difficult to escape the conclusion that in the present case the examination of the patent application was perfunctory, and the allowance of the claims necessarily of dilute, if of any, significance beyond that commanded by the statute. The applicants rested on merely differentiating what was cited to them. They never affirmatively identified their new, useful and unobvious advance over the prior art as distinguished from merely pointing out differences in detail between their device and those of the prior art. If anything, the prosecution, as far as it was carried, indicated that there could well be some patentable subject matter present without in the least relating that broad possibility to any of the particular inventions claimed in the 33 claims that were allowed, and, specifically, without relating that possibility to the claims here in direct controversy.

V

The nature of the claims of the patent and, indeed, the patent as a whole are best understood in terms of the nature of the task to which the device of the patent was addressed. While the patent is not, of course, restricted to pari-mutuel betting at race tracks using TIMs with numbered keys that are depressed to register a bet and which issue betting tickets automatically, the system of the patent is hardly a general purpose system. Its utility would necessarily be limited to counting situations fairly close in kind to that at race tracks. The role of the computer COMA, which, as it happens, is not involved in any of the claims in question, is not integral in any very substantial sense to the system elaborately described in the specification. The system of the patent is primarily an aggregator system, aggregating the number of wagers placed on each entry in the race in two separate aggregators, the registers MEMA which aggregate the wagers on each horse in the race in each of the three pools (i.e, win, place and show) and the TIM aggregator (the TIM memory WM), where the number of wagers made at each TIM on each horse in each of the three pools is separately aggregated. These are kept up to date, as each additional wager is signalled, by the updater, which, in each case, is a unit adder that is, it adds one. The task, then, is a very simple one, and it is the same for every race every day. There is no general purpose problem here calling for complex programs, and programs that must be altered from moment to moment or from day to day. Rather, the task is one that calls for a simple, stable system emphasizing high reliability and speed. The computer, too, has, as computer tasks go, a very simple

job, and that is to draw from the aggregator MEMA the total wagers in each of the three pools and the total wagers on each horse in each pool, to use these sums to compute the odds on each horse in each pool and the total wagered in each pool, and then to feed to the output display boards the result of the odds computation on each horse in each pool and the total bet. This the computer was to do each 70 seconds, and it had to have within it sufficient stored programming so that it could reach each register in the aggregator in order to read out the data in it for use in the computation. Such a task is without any inherent difficulty, and it involved no great degree of solid-state electronic data processing art. The whole Raceway task, when outlined to Mr. Leonard by Mr. Lynch at the very beginning of the project in 1959, seems not to have been thought to present any particular problem. There was no delay in Mr. Leonard's presenting confidently a system that would deal with the matter effectively.

Even a simple task involves a good deal of detailed circuitry. That is the present case. Perhaps Annex A will help in the visualization. This very untechnical sketch eliminates much of the wiring but does show the elements directly involved in the system of the patent. Very roughly the boxes at the left from TIM N at the top to the output units at the bottom show the flow of input data from the TIM to the display boards. Very simply, the task is to get the wagers placed at the TIM recorded in the registers MEMA and the TIM memory WM, to keep the wagers up to date in each race, to compute the odds every 70 seconds for display purposes, and at the

end to compute the payoff on the three pool winners. The boxes at the right are those which have to do with the control and driving of the system. They include all of the error checking components and the devices which furnish critical signals to latch and unlatch the keys on the TIM and which (and this is of course very important) make sure that all of the TIMs are searched for their data. As the patent makes plain, the various devices used are all familiar ones. They involve very detailed circuitry painstakingly worked out, but there is no novel circuitry involved as is clear from the face of the patent and from the trial evidence.

VI

In characterizing the claims in suit, plaintiff has styled the subject matter of Claims 20 through 22 as the totalizator system invention, Claim 23 as the non-allowed runner subsystem invention, Claims 24 and 25 as the TIM scanning subsystem invention, and Claims 26 and 27 as the erroneous data checking subsystem invention.

Claim 20 would seem, loosely, to claim the combination of a plurality of conventional TIMs, means of collecting from the TIMs and despatching into the system the betting data on each entry and identifying those data to the originating TIM, and means of aggregating the wagering data and sending an acknowledgment signal to the TIM so that it will stamp up and issue a ticket with the wagering data on it. If reference is made to Exhibit 11, it will be seen that the patentee identifies the TIMs as TIM 1 and TIM N, typical of a plurality of TIMS. He also identifies (Exhibits 11, 11A) the generating means for generating signals representing the wagered entry and the TIM as the step pulse generator, the scan counter and decoder, the entry register, the storage address generator, and the aggregator address transmitter as well as the buffer. Finally, the transaction calculating means for performing a calculation on the generated signals and transmitting an acknowledgment signal (when appropriate) to the TIM, so that the ticket will issue, is identified as registers MEMA, updater UAA and amplifier AKA. Cutting through, the system of Claim 20, then, comprises a set of commercially available fairly

standardized TIMs, appropriate electronic linkage between the TIMs, an aggregator, a unit adder, and an acknowledgment-signal amplifier between the unit adder and the TIM so that aggregating the wager effects an electromechanical release of the betting ticket.

The claim is strikingly barren of any genuine specification of means. Only by reference to Claims 21 and 22 does it become clear that the "calculation" of Claim 20 element (C) is the aggregation of the wagers and storage of them through the updater UAA and memory MEMA. The claim relates only to the simple operation of depressing one wager key on a TIM with the effect of actuating the updater to increment the register MEMA by the number one and effect, by return signal, an automatic release of a receipt or betting ticket. The detail of the circuitry, outlined in Exhibits 11, 11A by the heavy lines, and described at Tr. 170-179, 185-208, evinces no novelty. Each component is, as the specification makes plain, a familiar of the prior art (existing in various forms), and it performs its familiar role in a familiar way. The undertaking of the combination is an easy one, aggregating wagers without losing track of the horse on which and the pool in which the wager was placed, or the TIM at which the wager was placed.

The obviousness of the system is most readily seen in Annex A. The combination of means presented by Claim 20 is an utterly simple aggregator of punched-in data. Every component is in its predictable place and does its — in this field — simple office simply. The TIMs (Column 11, lines 43-67) are described "as of the type which" (line 43-44), and the record is clear that such TIMs were articles of commerce. The buffers are rudimentary; essentially "or" gates, each is wired to one of the keys (1,2,3 * * * n) in each TIM, and they pass the wager pulses to the entry registers (Column 11, lines 68-72). The entry register may be a plurality of flip-flops (Column 14, lines 9-24) of the kind already described (Column 12, lines 32-35) and as described in Richards, Arithmetic Operations in Digital Computers, Exhibit K, p. 48. Such use of flip-flops as registers was rudimentary, and is described in Richards Digital Computer Components and Circuits, 1957, p. 28 (Ex. 145; the Richards text is cited in the patent, Column 13, lines 34-35). The progress to the storage address generator (SAGA) and aggregator address transmitter (AATA) is, again, conventional (Column 7, lines 12-24, 41-46, 49-52; Column 14, lines 59-72, Column 15, lines 1-9). Both are, essentially,

"and" gates, at least in simplex operation, requiring a coincidence of the GERA signal and the entry signal in the case of SAGA, and, in the case of AATA, the coincidence of the AADR signal from SAGA and the SADD signal — the GERA and SADD signals are time-separated (D-7) signals from the control KA. The GERA and SADD signals simply reflect the result of the error test routine and derive ultimately from the step pulse (STP), scan counter (SKA) and decoder (DEC) circuitry that links into the system of Claim 20. The signal from the aggregator address transmitter (AATA) selects in the "memory" the multiplane magnetic core matrix (MEMA), the row and column which has in store as its "word" the number of wagers theretofore made at the TIM under scan on the horse selected and effects a "read-out" (MOA) to the updater (UAA) which adds "one" to the number part of the read-out "word" and restores it (MIA) to its row and column in MEMA and simultaneously despatches through the amplifier AKA a signal (ACKA) which as an "acknowledgement" reaches the TIM through mesne circuit paths to unlatch the depressed wager key in the TIM, releasing the ticket which is imprinted by simple electromechanical means in the TIM in the usual way (Column 8, lines 2-32, Column 13, lines 1-22, 52-62,

40-44). As the specification states, "Such recirculation type magnetic core matrices are well known" (Column 13, lines 32-33), and the updater (UAA) is a unit adder "and many are available in the present art" (Column 13, lines 52-53), and the specification refers to the two Richards texts. The particular chapter of "Digital Computer Components and Circuits" is not in evidence but the History and Introduction portion of the text (Exhibit 145), particularly pp 27-32 and Fig. 1-3, demonstrate the conventionality of the Claim 20 system.

If Claim 20 is narrowed to the specific figures and text of the patent it is necessarily a very narrow claim indeed, but in language it is extremely broad. If read in the first way, it is difficult to extricate the "means" elements of Claim 20 from the specification because the specification is written around the dual componentry and dual mode of operation and deals throughout with daily double wagering. If read broadly in obedience to its literal language, it inures as a statement of aims rather than as a workable statement of a union of identifiable means. But by either reading no unobviously new union of means is taught. In the striking language of Mr. Justice Matthews in Pickering v. McCullough, 1881, 104 U.S. 310, 318,

"In [the patentee's] apparatus, it is perfectly clear that all the elements of the combination are old, and that each operates only in the old way. Beyond the separate and well known results produced by them severally, no one of them contributes to the combined result any new feature; no one of them adds to the combination anything more than its separate independent effect; no one of them gives any additional efficiency to the others, or changes in any way the mode or result of its action. In a patentable combination of old elements, all the constituents must so enter into it, as that each qualifies every other; to draw an illustration from another branch of the law, they must be joint tenants of the domain of the invention, seized each of every part, per my et per tout, and not mere tenants in common, with separate interests and estates. It must form either a new machine of a distinct character and function, or produce a result due to the joint and co-operating action of all the elements, and which is not the mere adding together of separate contributions. Otherwise, it is only a mechanical juxtaposition, and not a vital union."

See also Anderson's-Black Rock, Inc. v. Pavement Salvage Co., 1969, 396 U.S. 57,

60-61, 163 USPQ 673, 674-675. So here, the system of Claim 20 represents a linear linkage of known devices each performing in sequence its familiar task. No discovery of any novel union of such means is present, but only a functionally adequate union of means in which each means is used to do what its nature and previous use suggest. The means combined in the system of Claim 20 neither embody nor obey any new law of cooperation.

Claim 21 adds nothing. (See Tr. 209-229) Element 21(A) simply identifies the matrix of "addressed," i.e., selectable or locatable magnetic cores carrying the bits making up the "word" that specifies and is specific to the aggregate wagers on one selection at one TIM — the registers MEMA. Element 21(B) is part of the idea of element 21(A); it simply specifies that the array of cores in the selected column and row will be such that it responds to the signal to MEMA. Element 21(c), similarly, signifies that read-out of the "word" to the updater UAA will occur in the form of MOA. Element 21(D) specifies the updater UAA. Element 21(E) identifies the signal path for MIA, the signal-set comprising the read-out word with its number part now increased by one, and the routine restoration of the word to its proper row and column of MEMA. Element 21(F) refers

again to the updater's simultaneously triggering the AKA unit to send out the acknowledge signal ACKA through the system — to the control KA, whence it issues as the signal CONA to the interface, where it becomes the signal CON and proceeds to the TIM to release the ticket. Claim 21 particularizes Claim 20. It adds nothing to the combination.

Claim 22 (outlined Tr. 230-237), like Claim 21, furnishes particulars of Claim 20, adding the circumstance that the second group of data comprised in the AADRA signals (the M + 1,2 * * *N set) passes from the storage address generator (SAGA) to the TIM address transmitter WATA (W = TIM) [as the first group of AADRA signals (the 1,2 * * * M set) passes to AATA], thence passes as the signal WADR to the TIM memory WM to effect read-out, as the signal WO, of the word reflecting the total wagers to that time at each TIM by selection, updates the number part of the word in the unit adder UAW, and restores the word, incremented by one, as signal WI to the correct location in TIM memory WM (Column 7, lines 18-24, 39-42, 44-46, 52-54, Column 8, lines 53-63, Column 13, lines 47-62). There is no "acknowledge" circuit. The specification seems, logically, to require essentially the same role of MEMA and

WM, and it was said at the trial (Tr. 234) that the MEMA and WM memory modules were interchangeable. (See Column 13, lines 11-18, 47-49.) The elements of Claim 22 disclose that WM and the immediately associated components comprise a conventional memory and unit adder used as a simple aggregator. See Column 13, lines 32-39, 47-49. Claim 22 adds nothing to Claim 20: the function assigned to WM in the specification makes it clear that elements (B) and (C) of Claim 20 can be taken to refer to the WM function no less than to the MEMA function provided the acknowledgement signal role is denied to the updater in the WM path. (Parenthetically, the TIM memory WM and associated updater UAW are not twinned in the system. The TIM address signal WADR to the TIM memory can emanate from whichever side is "master," A or B, i.e., from TIM address transmitter WATA or a presumed WATB. The AADR signal from the aggregator address transmitter AATA is, similarly, the signal from whichever address transmitter is master, but it is fed to both memories, MEMA and MEMB.)

Claim 23, the "scratch" subsystem, does not depend on Claim 20. As outlined (Tr. 237-247, Ex. 14, 14-A) by one of the patentees, the scratch subsystem provides a

set of steady signals (SKR1, 2 * * *N), initiated at switches, SKW1,2 * * *N, on the Console, C, to interdict the processing of wagers on those of the entries 1,2 * * *N which have been scratched; the interdiction is accomplished by using "a conventional equality comparator" (Column 14, lines 35-36) to generate an SKRI signal when a scratch signal, e.g., SKR1 (meaning horse 1 has been scratched) coincides in the comparator (TFSA) with a wager signal, e.g., H1N (i.e., horse 1 bet at TIM N) on the scratched horse; the SKRI signal functions to trigger a reject signal to the TIM and to "step" the scan to the next TIM. (Column 3, lines 41-45, Column 5, lines 3-20, Column 10, lines 34-51, 54-55, 59-61, 64-71, Column 12, lines 22-28, Column 14, lines 35-43.) The system, that is, comprises the conventional TIMs, a switch device to permit the emission of a set of steady scratch signals, a conventional comparator to match scratch signals with signals for attempted wagers on scratched entries, rejection signal circuitry and the acknowledgement circuitry of Claim 20(C). The idea of the system is simple; the simplicity is not that of discovered but of obvious simplicity, and the means invoked are an obvious dictate of the simple end sought.

The claim does not in reality go beyond the obvious teaching of the use of a com-

parator as a guard against taking wagers on scratches. The comparator compares the scratch signals with the wager signals and, in the case of coincidence, sends out a signal. That signal is used to trigger the reject and step impulses. Element (B) says nothing. It is an unreal multiplication of words. Switches do not "generate" "signals"; they make and break electrical contacts or paths. What must be meant is that there should be a key or switch for each runner number which when closed, completes a circuit that sets up the identifying signal for a particular runner number in the comparator. But that much is of the essence of a comparator's existence. Comparators exist to compare signals for identity or difference in a variety of ways (some of which can be gleaned from the excerpts from the British patent (749,836) cited by the Patent Office, bearing in mind that the signals involved in the British and the present patent are binary numbers encoding numerical and verbal information; the HSB and RCP elements in the British patent are comparators). The comparator reflects the result of its comparison in a signal and that signal, of course, can be used to do the obvious, to step the scan to the next TIM, or to unlatch the depressed key on the TIM without issuing any ticket, or both.

Element (E) is not really part of the

system claimed in Claim 23, and the awkward indication of the (E) trace on Exhibit 14 as going around the memory MEMA and the updater UAA, but through the amplifier AKA, discloses that embarrassing fact. The "system" of Claim 23 is devoid of means for *generating* an acknowledgement signal, or of means for aggregating the wager that is to be acknowledged because and only because it is correct to aggregate it. A glance of Exhibits 14, 14A explains that the scratch comparison and rejection system are upstream of the entire transaction calculator TCA; the scratch comparison and rejection are part of the transaction processor MRA activity, and, logically, must precede the TCA functions in real time so that the false wager is not aggregated in MEMA and WM.

The patentee Weida outlined Claimed 24 (Tr. 249-262, Exhibits 15, 15A) with reference to TIM scanning when no wagering transaction is being made at the TIM. It should be noted that, strictly, Claim 24 and its dependent Claim 25 are the only ones of Claims 20-27 in which the plurality of the TIMs is significant in the claim. The subject matter of the other claims is not related to the plurality of the TIMs. Column 1, lines 51-69 describes the object of the system so far as concerns Claims 24 and 25: to provide

a high-speed scanning means for interrogating a plurality of relatively slow-operating TIMs. "Scanning means" select the TIMs for interrogation sequentially. Interrogating means transmit an interrogating signal (SCN1A, 2A * * *NA, Col.3,11.48, 49) to the selected TIM, and, if the TIM is ready for a transaction it will transmit a selected transaction signal (H1N, H2N * * * HNN, where TIM N is scanned). Means sense for the transmission of the selected transaction signal, and, if none is sensed, that causes the scanning means to step to the next TIM and interrogate it. Provision is made to insure that the high-speed scanning means does not, by returning to make a second scan, cause a "redundant" second processing of the selected transaction signal (as to which see Column 10 line 72-Column 11 line 34).

An initial signal (ICL) presets the scan counter SKA to 1 (Column 3, lines 58-61); the scan counter SKA is a chain of conventional cascaded binary counters, as shown in Richards, Arithmetical Operations in Digital Computers, pp. 194-197, Exhibit L (Column 11, line 74-Column 12, line 7); the output of the scan counter SKA is fed as the SKNA signal to the scanner SCA (Column 3, lines 61-64). That scanner is a decoder which decodes the set of "1"s and "0"s from the scan counter SKA; the scanner may be

of the kind shown in the same Richards text, pp. 71-75, Fig. 3-3(a), Exhibit M (Column 12, lines 8-21). The scanner SCA decodes the SKNA signal and feeds it to the interface of the TIM and under scan as the signal SCNNA, the second N being the identifying number of the TIM under scan (Column 3, lines 64-67). The keys of the TIMs, when depressed, close switches, each key and its switch representing a runner, and one side of all the switches being connected to a common conductor; the signal from the scanner (e.g., SCNNA) connects to the common side of the switches, and, if one switch is closed (and, absent a defect, only one switch can be closed at a time), the scan signal crosses and issues from the TIM as a "selected transaction signal" (e.g., if from TIM N, as one of H1N * * * HNN). See Column 3, line 67 to Column 4, line 17. If none of keys of the TIM has been depressed — no wager is being made at the instant of scan, (and this is ascertained by the control KA's probing the "transaction-made" unit BMA with the TFB signal from the "1" output of the TFBF flip-flop (Fig.3)) — the scanner is stepped along to the next TIM (see Fig.2, at right, Fig.3 at top). See Column 4, lines 35-45. So too, if, by error, the key for a scratched entry has been depressed, the scratch circuity produces a signal at the

"or" unit 01 (Fig.3) which steps the scan to next TIM. See Column 5, lines 13-18. (The reiteration of the scan signal as a result of the false entry test is not significant here - Column 6, lines 21-30.) When a wager has been processed and error tested to the point at which the CONA signal is generated at the flip-flop CONF (Fig. 3) and has cleared delay unit D3, it effects, in transmiting the "or" unit 01 (Fig.3), a "step" of the scanner to the next TIM (Column 6, lines 53-62). The confirmation circuitry, of course, unlatches the depressed wager key in the TIM and issues the bet ticket (Column 8, lines 29-32). (The N + 1 check is not involved in Claims 24-25, Column 8, line 67 to Column 9, line 19). The "step" signal STEP is generated, as explained at Column 10, lines 54-71, when there is no error and when *no* CONA signal has been generated through processing a wager to validation and the issuance of a bet ticket: it is done when no wager signal is sensed or a wager on a scratched entry is found in the system. To be short, as Fig.3 illustrates at upper left, the scan steps when "or" unit 01 receives either (a) a signal that no bet has been made (BMD'), or (b) that the wager signal is on a scratched entry (SKR1), or (c) a valid bet has cleared the system to ticket issuance with the evolution of the CONA signal within the control KA of the transaction

processor MR (Fig. 2, right, Fig. 1A, left, Fig.3, left center). (The fourth signal at "or" unit 01, ICL, is not here relevant. It appears to function as a general system-starter (Column 3, lines 58 et seq.).) Finally the scan is prevented from re-scanning a TIM while the system is still in process of passing a "confirm" or "reject" signal to that same TIM by interposing an "and" unit A10 connected to the "do *not* confirm" and do *not* reject" outputs of the confirm and reject flip-flops (Fig. 4, center, "CONAF" and "REJAF") and feeding and scan signal SCN1A (SCNNA) to the same "and" unit A8 so that it clears the interface IF (IFN) only if neither a confirmation nor a rejection is in transit through the system. This follows from the datum that, when the SKRI and CONA trigger the STEP signal, they also (mediately) function to set the REJAF and CONAF flip-flops respectively to "1" (via "and" units A 92 and A 90, Fig. 4). During that period the TIM originated BID1 signal is operative. After the key and ticket release (or key release only) is triggered, the BID1' signal sets to "0" the CONAF or REJAF flip-flop (whichever had been set to "1" because of a confirm or reject) thus providing the missing signal for the coincidence of signals required to clear the SCN1A scan signal through the interface to

the TIM as interrogation signal SCN1 (SCNN).

Again, the subsystem claimed combines conventional components to perform a familiar assignment in a conventional way. Claim 24 commences with the plurality of commercially available TIMs as element (A). The operational language of (A) means simply that when a TIM wager key is depressed, it closes a circuit switch; that closure completes a circuit leading from the TIM via one or another of the buffers (all "1" keys leading to buffer "1," all "N" keys to buffer "N") to the transaction processor MR, and, specifically, to the entry register, 1HRA, Fig.2. The scanning means of claim element (B) which interrogates the TIMs in order is the conventional binary counter which emits the SKN signal and which is stepped by return signal from the system, closing the impulse sequence by stepping or advancing the scan counter SKA. The interrogating means of element (C) is the scanner or conventional decoder SCA which decodes the signal SKN and transmits it as (for example) the signal SCNNA to the interface IFN which transmits it to the TIM where it, in effect, becomes the wager signal and proceeds into the system. The sensing means of element (D) for sensing a wager signal is the BMA unit in transaction processor MRA (Fig.2), and is an evidently

simple logical element (Column 14, lines 29-34) made up of "or" units and an "and" unit. The stepping means of element (E) which is to function when the *no* wager signal (BMD') is present, is the "and" unit A1, the "or" unit 01, and the step pulse generator (Fig.3) and binary counter SKA (Fig.2).

No discovery is present here. Detail abounds, but ingenious novelty is not present. It is pedestrian circuitry that accomplishes its very simple goal of furnishing a pulse that tracks through a system (with the functions of which scanning is not concerned) and, on circuit completion to origin, ticks the binary counter on to the emission of its next count signal.

Claim 25 adds nothing. It simply covers the other alternative — that a wager has been made — and it requires that a stepping control exist so that the scan does not step to the next TIM before the bet has been processed. The claim is ineptly phrased, for to specify "means for processing a selected entry transaction signal sensed by said sensing means [of Claim 24(D)]" is to call for a means of limitless dimensions, irrelevant to the nature of the claim. (The patentee outlined the claim at Tr. 262-272.) The point of the claim is to add to the elements of Claim 24 the element of means to delay the step-

ping of said scanning means to select the next TIM until any selected transaction signal sensed by said sensing means has been confirmed as a valid wager or rejected as an unallowed transaction. The added means of Claim 25 are, of course, not the whole data processing system, as Exhibits 15, 15A suggest (cf. Tr. 265), but the fact that the CONA, BMD' and SKRI signals alone directly STEP, and REJA does so mediately. The consequence of that is that in the case of a duly processed wager, the Step pulse generator (Fig.3) is not energized, to move the scan counter SKA on (Fig.2) to issue a new SKNA signal to the scanner SCA to initiate the new SCNNA, SCNN sequence through interface IFN to TIM N, until the CONA signal is at least despatched to interface IFN, and there generates the CON signal that releases the wager ticket.

Claim 25, the rest of Claim 24 in reality, is equally obvious, the same detailed and uninspired circuitry doing the routine routinely. Neither Claim presents anything except a rudimentary scan system, nothing approaching the versatility of Schrimpf, No. 3,029,414 (Exhibit 3A), passed over so lightly in the office action. It is not possible to conceive that Claims 24 and 25 could have survived the prosecution if the Patent Office had examined the claims with the required particularity.

Claims 26 and 27 (Tr. 272-286, Exhibits 16-16A), are addressed to one of the error-checks incorporated in the total device. They parallel Claim 23, which dealt with the check against wagers on scratched entries (Tr. 289). The entry checking means is the "two entry transaction" unit THBA of Fig. 2, located in the transaction processor MRA; it "can be a conventional majority logical element" which generates a signal THBI if the entry register (1HRA) emits wager signals on more entries than one (Column 14, lines 44-56; the Boolean equation [correctly given in Exhibit 2, p.35, lines 15-16] means simply that if the signal TFT coincides with the coincidence of wagers on any two or more entries, the THBI signal is generated.

Again, the Claim element 26(A) is the commercial TIM as in Claim 23. Claim element 26(B) speaks of "entry checking means" for detecting erroneous wager signals and thereupon transmitting a rejection signal to the TIM. Claim element 26(C) is the acknowledgement means as in Claim 23(E). The patentee visualized the subject-matter of Claim 26 (or, perhaps, of Claims 26 and 27) as the flagging down of "two horse bet" situations and of false wager signals originating within the system (Tr. 275-296, particularly 277-278).

The two claims relate to the second and fourth tests in the signal test routine schematized in Figure 3, the tests utilizing the flip-flops TFTF and RSCF. If the first test (test for bet made) verifies that a wager signal has been entered in the entry register 1HRA, the test-for-two signal TFT is generated in the flip-flop TFTF, and, through use of the two-entry transaction unit THBA (a conventional majority logical element), determines whether more than one wager signal has entered the entry register as a result of the scan of the TIM then under scan; if so, the THBI signal issues from the majority element THBA (Fig.2) and, in control KA, coinciding with the TFT signal in "and" unit A7 (Fig.3), passes "or" unit 03, sets the ERAF flip-flop to 1 and generates signal ERA, which, via "or" gate 04, sets the REJF flip-flop to one, generating (after delay at D4) the REJA signal that in the interface (Fig.4) is (along with scan signal SCNNA) a component at "and" unit A62 of the signal that sets the REJAF flip-flop to 1 and despatches the reject signal REJ to the TIM (Column 4, lines 49-74, Column 9, lines 57-62, 67-72, Column 10, lines 31-50). If there is no duplicate signal, THBI' initiates the next error check, the scratched bet check.

The routine then disposes of the scratch test, and, if the wager is not on a scratched

entry, the signal SKRI' (negating a scratch bet) energizes the 0 input of the scratch flip-flop TFSF and the 1 input of the RSCF flip-flop to commence the test for a false signal through the RSCNA' signal and its invert RSCNA, identifiable as "reset scan." The language of the specification is not very fortunate in explaining the false signal sequence, but apparently the first-functioning signal is the invert, RSCNA', the 0 output of the RSCF flip-flop. It initiates the test for the systemic validity of the wager signal being processed by being fed to *all* the interfaces, IF1 * * * IFN, and, necessarily reaches the IF of the TIM under scan, say, e.g., IFN, and terminates the generation of the scan signal SCNNA. No wager signal should then persist in the system since it is the scan signal that is fed out of the TIM as the "selected transaction signal"; "after a delay to permit the passage of signals through the loop," through the system including the TIM (Fig.3, D1), the RSCNA signal is fed from the 1 output of the RSCF flip-flop to the BMA unit (Fig.2) to test for the presence of a false wager signal in the entry register (note in Column 14 line 31 that the equation is satisfied, and the BMD signal is generated, if either the "test for bet signal" or the RSCNA signal coincides with a wager signal); if a wager signal is present

(and it should not be, since the invert RSCNA' has terminated the scan signal SCNNA), the BMD signal returned to the control KA at "and" unit A6 with the RSCNA signal (Fig.3) will feed through "or" unit 03 to the 1 side of flip-flop ERAF and generate ERA (which shuts MRA down) and, via "or" unit 04 will set the flip-flop REJF to 1, generating, via delay D4, the REJA signal (Fig.3) which (as before) via "and" unit A62 sets the REJAF flip-flop to 1 and despatches the REJ signal to the TIM (Column 5, lines 20-46, Column 6, lines 16-17, Column 9, lines 56-62, 67-72, Column 10, lines 31-51).

As in the case of Claim 23(E), relating to the test for non-allowed scratch signal, the acknowledgement means does not genuinely function as part of the error checking role of the combinations of Claims 26 and 27. To be sure, if there is no duplicate-wager or false signal or other error, the valid wager will be processed through ticket issuance. That, however, is not functionally connected with either the test-for-two or the false signal or the scratch error tests, but, rather, is functionally related to aggregating wagers. In the case of the "two-horses bet" error check, the check system is upstream of the aggregation and updating steps which alone can give rise to the acknowledgement signal. There is, then, no acknowledgement

means in functional union with the "two-horse bet" error checking means except in a more inclusive combination, not claimed, that would embrace the aggregation of the wager.

The "test for false wager signal" of Claim 26 is somewhat different; because of the obscurity of the explanation of the operation of the RSCNA signal and its invert (Column 5, lines 20-46, Column 6, lines 18-33, 47-56), the final result of the routine is puzzling. Figure 4 explains little in describing the path that RSCNA' takes to the "and" unit A8 to generate, if SCNNA and AMST coincide with it, the SCNN signal, if the BID1' signals are at the 0 inputs of CONAF and REJAF; that sequence can be related to the CON signal to the TIM via "and" unit A61 and to the holding effect described in Column 11 lines 11-39. But no integral combination of the false entry check with the acknowledgement means UAA and AKA (which are components of the distinct aggregation function) is present.

It may be thought that Claim 26 refers only to the false signal test (despite the explanation at Tr. 277-278) and that Claim 27 refers only to the plural wager signals error. The effect of the language of Claim 27 is to

substitute the means of Claim 27 for the means of Claim 26(B).

As in the ease of Claims 20 through 25 no discovery is disclosed, only painstaking articulation of familiar means to perform simple error checks through use of circuitry suggested by the nature of the tasks to be performed and the nature of the conventionally appropriate components that the tasks themselves pointed out as suited for the service.

The claims depend absolutely on exploiting the last paragraph of 35 U.S.C. 112, which has been said to have been intended to mitigate such holdings as that in Halliburton Oil Well Cementing Co. v. Walker, 1946, 329 U.S. 1, 71 USPQ 175, which dealt with the meaning and limits of the often expressed principle that in claim drafting the draftsman must not use "conveniently functional language at the exact point of novelty" (General Electric Co. v. Wabash Appliance Corp., 1938, 304 U.S. 364, 371, 37 USPQ 466, 469). In Halliburton Mr. Justice Black said for the Court (329 U.S. at 8-9, 71 USPQ at 178):

> "A claim typical of all of those held valid only describes the resonator and its relation with the rest of the apparatus as 'means associated with said pressure responsive device for tuning said receiving

> means to the frequency of echoes from the tubing collars of said tubing section to clearly distinguish the echoes of said couplings from each other.' The language of the claim thus describes this most crucial element in the 'new' combination in terms of what it will do rather than in terms of its own physical characteristics or its arrangement in the new combination apparatus. We have held that a claim with such a description of a product is invalid as a violation of Rev.Stat. §4888. Holland Furniture Co. v. Perkins Glue Co., 277 U.S. 245, 256, 257; General Electric Co. v. Wabash Appliance Corporation, supra. We understand that the circuit court of appeals held that the same rigid standards of description required for product claims is not required for a combination patent embodying old elements only. We have a different view." (Footnote omitted.)

The Court held the claim bad because it embraced every possible means that, in union with the other elements of the combination, already in the prior art as combinations, would emphasize the sought-for echoes. Mr. Federico (then Examiner-in-Chief, United States Patent Office) said in his Commentary on the '52 Act (35 U.S.C. pp. 25-26) in discussing the third paragraph of Section

112 and its relation to such cases as Halliburton:

"It is unquestionable that some measure of greater liberality in the use of functional expressions in combination claims is authorized than had been permitted by some court decisions, and that decisions such as that in Halliburton Oil Well Cementing Co. v. Walker, 67 S.Ct. 6, 329 U.S. 1, 91 L.Ed. 3 (1946, are modified or rendered obsolete, but the exact limits of the enlargement remain to be determined. The language specifies 'an' element, which means 'any' element, and by this language, as well as by application of the general rule that the singular includes the plural, it follows that more than one of the elements of a combination claim may be expressed as different 'means' plus statements of function. The language does not go so far as to permit a so-called single means claim, that is a claim which recites merely one means plus a statement of function and nothing else. Attempts to evade this by adding purely nominal elements to such a claim will undoubtedly be condemned. The paragraph ends by stating that such a claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof. This relates primarily to the construction

of such claims for the purpose of determining when the claim is infringed (note the use of the word 'cover'), and would not appear to have much, if any, applicability in determining the patentability of such claims over the prior art, that is, the Patent Office is not authorized to allow a claim which 'reads on' the prior art."

Much is certainly read into the third paragraph of Section 112 (see e.g., Kockum Industries, Inc. v. Salem Equipment Inc., 9th Cir. 1972, 467 F.2d 61, 175 USPQ 81; Application of Knowlton, C.C.P.A. 1973, 481 F.2d 1357, 1361, 1366-1368, 178 USPQ 486, 489, 492-494), but, of course, some workable means must be found in the specification (see, e.g., Application of Jones, C.C.P.A. 1967, 373 F.2d 1007, 1014, 153, USPQ 77, 82-83) in order to satisfy the critical requirement of Section 112 that the claims particularly point out and distinctly claim the subject matter which the patentee regards as his invention. Cf. Application of Bozek, C.C.P.A. 1969, 416 F.2d 1385, 1390, 163 USPQ 545, 549-550.

The structure and content of the claims requires examination in the light of plaintiff's key argument that, while Claim 20 is the most basic and inclusive (i.e., the least

limited in its range of reference), dependent Claim 22 is the most important, and that the most significant area of novelty centers around the "means" for generating signals representing each TIM's identifying number and the use of electronic data processing (EDP) means for aggregating TIM window bets — coupled with overall use of EDP means to service parimutuel betting at racetracks. Subordinately, it is argued that Claim 22 manifestly requires EDP means (since it uses the language of "memory," "addressed memory positions," "address-selection means," "reading out"), thus it is claimed, mandating an EDP reading of Claim 20. Plaintiff's Postrial Brief, pp. 7-8.

The last point is valueless. Hybrid systems exist. Deciding how many components to convert to EDP is a matter of informed choice.

Returning to the first point, plaintiff argues that "the novel TIM number signal generation means of Claim 22 provides for a synergistic result — the same TIM number signal generation means is used both for aggregation of the TIM window bets and for scanning of the same TIMs for betting data" (Post-trial brief p. 8). That is, the scan counter SKA ("a chain of conventional cascaded binary counters wherein each binary counter has an output from both its

'1' and its '0' sides such as those shown * * * on page 194 of Arithmetic Operations * * * by R.K. Richards * * * 1955"; Col. 11, line 74 to Col. 12, line 5) is the disclosed means of generating the TIM number signals, and, via decoder DEC ("similar to scanner SCA," Col. 14, line 75, which is a "decoder which decodes the combinations of "1's" and "0's" from the scan counter SKA," as shown on pages 71 et seq. of the same Richards book, Fig. 3-3(a), Col. 12, lines 8-21) and Storage Address Generator SAGA(Col.14, lines 59-74, see pp. 143-144 supra) produces the TIM address WADR, used to address the TIM memory WM so that the wagers on each TIM, can be aggregated. The scan counter SKA (the argument continues) also generates the scan signal SKNA fed via scanner (a decoder) SCA as SCNNA through interface IFN and thence as SCNN to TIM N, where it goes through the latched entry key switch to emerge as the wager signal (e.g., HNN). (Posttrial Brief p.8). Plaintiff's counsel explained the concept at the close of the trial (Tr. 3683-3687, 3729-3732; cf. Tr. 230-236): the SKNA signal travels a many-wired cable carrying (one binary "place" to each wire) a binary number — say, seven wires (eight?) to accommodate numbers up to 128 for 128 TIMs ($128=2^7$). The insistence is that the

synergistic element is in the manifold use of TIM number signal generation means of Claim 22 (that is element 20(B), which is picked up in elements 21(B) and 22(B)) to scan the TIM for betting data and to aggregate the TIM wagers, assuring the correct association of TIM and wager. Phrased somewhat differently the same argument is reiterated in Plaintiff's Reply Brief (R4-R9, R-14-R-15), and in Plaintiff's Proposed Findings of Fact etc. at F 107, F 111, F 113, F 114, F 119 and F 159, proposed findings 4.35, 4.4b5, 4.4b6, 4.4c11, last sentence, 4.4c12, and 6.21-6.23). Special emphasis is given to Claim 20(B) (generating means responsive to the wager signal to generate signals representing the entry *and* the originating TIM), and it is asserted that, while Claims 20-22 and 24-25 together define the body of the patented Tote, parent Claim 20 is its heart, Claim 20 (B)'s TIM number signal generation means is the synergistic link, and the Claim 22 invention is the most important. It is argued that Claim 22 recites the TIM window bet aggregation, using the TIM number signals (Claim 22(B), address-selection means for receiving signals "generated by said generating means" — the element 20(B) means — for selecting the particular memory position associated with the particular TIM). It is

asserted that TIM number signal generation and TIM window bet aggregation were new in racetrack lore and that the Claim 22 TIM memory WM is "most important" (Posttrial Brief p.6) because it includes the novel EDP elements of Claim elements 20(B) and 22(B). Novelty for all elements is claimed because they are "limited to * * * EDP technology." More seriously, it is asserted that the TIM number signal generation means of Claims 20-22 (Clause 20(B,) as well as the TIM memory WM (Claim 22, especially element 22(B)) "are completely novel over all the prior art" (R7).

Plaintiff's reading of the Claims puts strains on them that they cannot support. Strictly, Claim element (A) in Claims 20, 23, 24 and 26 is not genuinely a combinatorial element of the combinations of the claims. The systems of the patent (Column 1, lines 11-13) are "systems for processing data received from" TIMs. On plaintiff's own constant (and groundless) argument that the completely EDP character of the systems is one significant element in the patentable novelty of the systems in the racetrack field, the TIMs are outside the field of the inventions, for they are mechanical and electromechanical, and as slow as ever. And note Columns 15-16 of the summary, which treat the TIM, its

switches, etc. as apart from "A data processor * * * comprising" ten subsystems and subassemblies which are then described briefly but do relate back to the entire specification.

To provide a data processing system to a plurality of TIMs is not to present a combination that could be patentable, for as a combination it is, obviously, exhausted, and patentable novelty could reside only in the union of data processing sub-means, new, old or both, that as a data processing system or subsystem served the plural TIMs. That is, in reality the structure of the patent as a whole, despite the choice of claim form. To put it another way, the TIMs and their demands for service were not an element of the claimed inventions; they rather represented the job assigned to the systems technicians. Note Claims 1, 10, 15 and 17. (And, in passing, note that parent claims 2 and 3, easily resist the contention that they are totalizator rather than data processing claims.)

Apart from the skew given to Claims 20-27 by incorporating the TIMs in them as elements of the allegedly patentable combinations, the claim language itself does not support the constructions plaintiff seeks to impose on it. Specifically, the closing language of Claim 20 (element (C)) — "only if the transaction is correct" is null

language. It cannot import, as plaintiff now suggests, the whole set of error check subcircuits (described in Column 4, line 54 to Column 6, line 12, Column 9, line 57 to Column 10, line 54, Column 16, line 65 to Column 17, line 19, Column 17 lines 64 to 75, Column 18, lines 56 to 67), and it gains nothing from the license of the third paragraph of Section 112. The phrase indicates no means, and it states only a desideratum that is not the subject matter of the union of means of which the Claim is composed. Claim 20 deals with means for aggregating wager signals "representing" both runner and the TIM of origin, making a calculation on the signal, and acknowledging the wager to the TIM.

The generating means of Claim element 20(B) responsive to the selected transaction signal is identified by plaintiff as the scan counter SKA, the SKNA output of which is fed to the scanner SCA (a decoder) and another output of which is fed to the decoder DEC and thence to the storage address generator SAGA. It is invoked in Claim element 21(B) and Claim element 22(B). Claim 21 identifies the components of the aggregator centering on the memory MEMA and it represents ABC data processing. "Memories" have to be thus and

thus implemented; the very term implies addressed positions for "words," retrieval of them for arithmetical calculations, and return of them to the addressed position. Claim 22 is precisely the same except that it refers to the simpler aggregation centering on the memory WM and involves no acknowledgement signal.

The claimed "synergistic" effect is not present. Annex E presents in stripped down form the components and circuit paths involved. Because of the daily double language that entangles the specification, the signal generating effect of BID1 is not made clear; depressing a TIM key definitely energizes a corresponding line to produce a signal on that line in correspondence with the latching key that has been actuated (Tr.188) and that signal must be BID1 (Col.3, lines 67-72, Col. 6, lines 59-63, Col. 11, lines 11-32). Beyond the bare word "decode," nothing of the word-forming function of scanner decoder SCA and the decoder DEC is made explicit. Since, however, the signal from SKA is a simple number in binary numeration, the same signal must be fed to both decoders SCA and DEC.

The output of SCA, is the scan signal SCNNA which issues from the TIM interface IFN as signal SCNN crosses the closed switch in TIM N "and is fed out as a

selected transaction signal" (e.g., HNN) (Col. 4, lines 7-8), goes through the buffer for horse N and enters the entry register 1HRA. The entry register is or may be a plurality of flip-flops, presumably one for each possible entry (Col. 14, lines 9 et seq.); that would mean that, if there are only ten keys on each TIM, there would be only ten flip-flops in the entry register 1HRA, and the entry register could be wired directly to the ten buffers through a ten-wired cable, and the buffers similarly wired through such another cable to the "selection" side of the ten transaction selection switches in the TIMs. The signal that is "fed out" of the TIM to the buffer as the selected transaction signal would appear simply to "pass through" the buffer (essentially an "or" unit ready to pass a wager signal from any TIM on the entry it handles, Col. 11, lines 68-72) without modification and without providing any information about which ticket machine generated it; and it appears to reach the entry register in the same signal form it had when it left the TIM. At the entry register it is simply a voltage (Tr.1337, 1341, 2770-2775, Exhibit 152).

One input to the entry register is the STEP signal (which also advances scan counter SKA and, hence, produces signal

SKNA). The STEP signal "clears" the entry register 1HRA (col. 6, lines 63 et seq.) and at the same time, evidently, sets the TFBF flip-flop (test-for-bet) to 1 and the CONF, REJF and GERF flip-flops to their "0" state.

The other input to the entry register (which has been "cleared" by the STEP signal) is the simple voltage of the selected transaction signal originating in the TIM under scan, which sets the chosen flip-flop to its "1" state. The "1" output of the flip-flop involved "is connected to one of the 1HRN signal lines" leading to the storage address generator SAGA (Col. 14, lines 14-15). It would seem, then, that when the selected transaction signal leaves the entry register 1HRA, it is not a compound signal identifying both entry and TIM. In any event, the role of the storage address generator SAGA, is, at minimum, to compound the signal by adding the TIM - identifying information derived from the companion decoder DEC (Col. 7, lines 11-17) to whatever, if any, wager identification is implicit in the HRN signal from the entry register. SAGA is a set of "and" units (apparently one for each possible entry) requiring a coincidence of a selected transaction signal, a DKN signal (identifying the TIM) from decoder DEC and a GERA signal (Col.7, lines 12-17, Col.14, lines 63-74).

Since the signal is to be stored in the memory MEMA by TIM *and* by entry, the address of the signal is complete and it moves on under the GERA impulse (another derivation of STEP) as the two group signal AADRA (see Annex F for detail) to the address transmitters AATA and WATA. The address transmitter AATA (in simplex operation) would appear again to be a set of "and" units requiring the coincidence of the compound AADRA signal with the SADD signal (another, but delayed, derivative of STEP); the address transmitter WATA seems to be similar, requiring a coincidence of the SADD signal and the group 2 segment of the compound AADRA signal; the means of dividing the signal (if that is necessary) are not explained (Col. 15, lines 1-20).

The result is the storage and updating of the complete data in the aggregator memory MEMA and the making of an updated record of the number of wagers at each TIM in the TIM memory WM.

The assertion of synergistic effect evaporates with the observation that the decoder DEC supplies the TIM number to the storage address generator SAGA for inclusion in the address of the pending selected transaction signal which is then

stored in two memories; it is stored in MEMA by entry and TIM, and it is stored in the dubiously useful WM as a register of the total number (unsorted) of wagers at each TIM. No unobviously useful economy exists in employing scan counter SKA as such a signal generation means as it may be to feed both the scanner (decoder) SCA and the decoder DEC. If a second memory was to be used to store some of the same data being stored in MEMA, obviously it would be done by the same means at the same take-off point. That was the role of the DEC reading of the signal from SKA. A special ingenuity of indirection would be required to do it any other way. SKA is actuated by the omnipresent STEP signal of the step pulse generator STP which is, apparently, in the real time scheme of the system, the significant impulse generator in direct and derivative forms at the scan counter, the entry register, the storage address generator (through the GERA signal), and the address transmitters (through the SADD signal). The two decoders SCA and DEC, evidently, decode the same signal in different senses for use at different stages.

The TIM memory WM does nothing that a mechanical counter on the TIM could not do as well, and, moreover, the TIMs in use at the time in New York were required to and did maintain a separate print-out of all transactions, an electro-mechanical or electrical and mechanical operation of familiar sort (Tr. 1841, 2264-2269). If there was a use for the TIM memoray data, reading them out of the more elaborate data required to aggregate and update the wagers in the registers of the memory MEMA was another way to do it. The allegedly "synergistic" effect is, then, the common attribute of all EDP systems — that they are energized from a common source and are ordered in real time by a common step signal.

VII

The prior art emphasized at the trial and considered in the posttrial briefs and proposed findings is all but confined to totalizator systems and patents. While it has been concluded on the face of the patent and in the light of the disclosures of its cited materials, that the claims in suit do not embrace any patentable discovery or invention, and it has been concluded that the relevant field for inquiry is data processing, of which racetrack parimutuel totalizators are instances, consideration of the totalizators of the prior art confirms the conclusion that no patentable discovery or invention is present.

The prodigious detail involved in discussing the totalizators of the prior art gives

them a specious appearance of difficulty and complexity. They are indeed detailed as they must be, but straightforward. The block diagram, Exhibit BL, generalizes the parimutuel data processor in terms of a sequence starting with the wager placed at a TIM and proceeding through pickup of the wager data in a scanner stage, validating and testing it in a processor stage, aggregating the wagers in the first phase of a transaction calculation stage, performing calculations on the data in the odds, etc. calculator, and displaying the result. Feedbacks from the processing and aggregating stages are shown — a "reject" feedback for erroneous transactions from the processing stage and an "acknowledgement" feedback from the aggregator stage, signifying that the wager has been recorded and a betting ticket will be released.

Handley No. 2,479,681 (1944, 1949) (Exhibit BQ), not cited in the Patent Office, is easiest seen in Exhibits BQI and II, which enlarge and display in one sheet the seven figures of the patent; each of the patent figures is a segment of a single schematic diagram. BQI outlines in red the principal components of the system, and BQII is the same set of figures color coded to trace out the history of a 10 shilling wager that Horse No. 1 would win and Horse No. 2 place second. Exhibit BS shows Handley in functional or block diagram form.

Starting at upper left of Exhibit BQII, the yellow line shows the shilling stake key depressed; below that the upper blue line shows the 1F key depressed for Horse No. 1 to win; and the next lower blue line shows the 2 key depressed for Horse No. 2 to place. Depressing the wager and stake keys rotates counterclockwise the three interconnected cams 35 (CMC, OPC and TCC) until the tooth on cam OPC is caught by the latching pawl just when the knob on control cam CMC is at topmost and rides the guide to its high point; that action closes contacts (seen just above CMC) CM 2,3,4 and 5 and opens contact CM1. Closing CM3 generates a TIM bid signal, shown by the brown line, which goes to the right, up through changeover contact points and reaches the commutater, which performs the scanner office in Handley. The commutator or scanner disk or wheel has on it five concentric rings. The two outer rings are divided into as many radial segments as there are TIMs in the domain of the scanner; each segment is wire connected to a different TIM. The three inner rings are wire connected into the common data processing system. Brush contacts on a rotatable bar, seen as extending vertically upward from the center of the commutator, provide selective electrical

connection between the two outer and the three inner rings. Rotation of the bar connects in sequence each TIM that is ready with a bid signal to the common data processing system. The bid signal (brown) reaches the outermost of the rings, crosses on the bar to the outermost of the inner rings, and thence reaches and energizes the coil of the solenoid LM which slows the commutator bar at the scanner or commutator segment allotted to the TIM making the bid signal. The commutator then returns a "connect" signal CN (traced in purple) to the TIM; the signal (purple) travels from the innermost of the rings to the inner of the two outer rings of the scanner at the segment allotted to the TIM under scan, thence travels via changeover relay contact 6 through now closed contact CM-2 in the TIM and finally through contacts TC-1 and RN1 to energize the relay OP, the "connect" relay. (The RN relay at upper left, the energizing of which closes contact RN-1, functions in the central control's check to assure that the TIM operator has set his TIM for the correct race and the correct number of entries.) The energizing of the OP relay closes contacts OP-1, 2 and 3, shown along the dotted purple line, launching the stake signal (yellow) and the two selection signals (blue) into the system. These signals are simply voltage. Contacts OP4 and 5 (well below OP1, 2 and 3 and

offset to the left) have also been closed when relay OP operated (as well as OP6, still lower and further left on the bottom line, the closure of which completes a path to the TIM for a rejection signal). Closing contacts OP4 and 5, connected to the TC or "acknowledge" relay, prepares a path for the acknowledgement signal (outlined in green). The blue wager signals go to the relay 38 (a pair of relays, A and B) and the stake signal goes to the relay 32 (A and B) at the lower far right.

At the far upper right ("1 and 2 combination counter") 39 is the aggregator for the win and place combination wager. The dual relay 38, energized by the blue wager signals, closes the contacts off to the right of them, preparing paths to aggregate the pending combination wager. The dual relay 32 at lower right, energized by the 10 shilling wager signal, closes switches which send two signals each (4 plus 6 shilling signals) to the win and place aggregator and to the total aggregator. The signals energize solenoids which close the 2 and 3 switches in each aggregator and send out on the green signal lines the two pairs of acknowledgement signals, which, ultimately, reach the TIM's ticket issuing and unlatching mechanism at far left. Enroute, at a point to

the right of the scanner or commutator, the signal lines reach a pair of changeover keys, CCR, the operation of which enables a choice between sending the signal from the combination counter or that from the total counter onward as the acknowledgement signal to the TIM. (The relays RC and AC, to the left of the changeover keys CCK, are actuated by the ACK signal from, respectively, the combination counter and the total counter.) The chosen acknowledgement signal passes through changeover relay-contacts 3, 4 (at changeover relay WC) and relay contacts 26, 27 (normally closed contacts related to the test key T just above 26, 27) and thence passes through the "operate" relay contacts OP4, 5, which at this time are closed, to energize the TC relay coil, closing contacts TC3, 4 to ground and to voltage potential.

The "connect" signal CN (purple) meanwhile, energizing relay OP, has turned cam OPC counterclockwise slightly; the latching pawl releases and the pawl's vertical member arrests against the second tooth on the cam. When relay TC is energized by the ACK signal, the contact TC1 opens, de-energizing the OP relay and causing contacts OP1, 2 and 3 to open, terminating the stake (yellow) and selection (blue) signals from the TIM. Contacts OP4, 5 of the ACK circuit (green) open as well, as

does OP6 in the (red) reject circuit, so that their signals, too, are terminated. Contact TC2 in the bid (brown) circuit is opened as an effect of energizing relay TC, breaking the brown bid circuit and terminating the bid signal from the TIM. The TIM, in result, is disconnected from the data processing system. The TC relay is still operating, having closed the contacts TC 3, 4, connecting across it from negative potential to ground.

Termination of the bid signal (brown) from the TIM to the commutator or scanner de-energizes the solenoid LM, and that allows the scanner bar to resume its scan and step to the next TIM ready with a bid signal.

The ACK signal, when it de-energizes the relay OP and opens contacts OP1, 2, 3, also occasions a further rotation of cam OPC and, under the influence of relay TC, the latch on cam TCC is lifted clear of the tooth on TCC and the set of cams completes its rotation. The rotation of control cam CMC trips the large PC latching pawl, permitting the contact PC to close, setting the printing and issuing solenoid to print and issue the wager ticket. The rotation of control cam CMC opens the contacts CM 2 through 5, and, specifically, by opening contacts CM 4

and 5 interrupts the ACK holding path, completing the TIM's disengagement.

Protection of the system from wagers on scratches is provided by manipulating the scratched entry's lever in the bank of non-runner control levers (NRC); that action automatically rotates the MNCS switch to adjust the system circuitry to the reduced number of runners. Throwing a scratch lever energizes the relay located directly above it (1NR * * * 6 NR), and each such scratch relay has to its right, under the cancel relays, contacts 5 and 6, connecting to cancel relays A and B respectively. If a wager on a scratched horse is made, either on the upper or lower selection signal line (blue), then the corresponding contact (5 or 6) will open, breaking the wager signal line (blue) and energizing the corresponding cancel relay above it. That energization will, in turn, close the corresponding cancel contact to the left (Al or B1), sending a reflex signal to the TIM via change-over contact 2 and across contact OP6 to the cancel solenoid. Operation of the cancel solenoid engages the solenoid latch with the lower tooth on the control cam CMC and rotates the cam set so that the guide atop cam CMC drops, opening the CM2 through 5 contacts, terminating the bid (brown) and connect (purple) signals; that de-energizes the OP relay and opens the stake and wager con-

tacts OP1, 2 and 3, aborting the attempted wager and resetting the TIM. No ticket is stamped and issued because control cam CMC does not complete tne counterclockwise rotation that actuates the printing and issuing solenoid.

Handley includes circuitry, outlined in orange, to protect the system against repugnant dual runner or dual stake signals. The relay RG (runner guard relay) in the transaction processor section relates to mistaken dual runner signals and relay SG relates to mistaken dual stake signals. The relays are energized if more than the "measured" current appropriate to a runner or stake signal appears on the runner (blue) or stake (yellow) signal line. [Note that in each stake cell (28-34) at bottom right a resistance (R 7-9, 11, 12, 14, 16) imposes "measure" on the orange stake guard signal; and that, upper right, the three runner cells exhibit resistances imposing "measure" on the runner guard signal (orange). Relays RG and SG normally are not energized by the signal strength measured to them. A normal runner or stake signal will only balance out the normal guard signal to RG and SG. Hence, if one runner (at relay 38) and one stake signal (at relay 32) close contacts to their respective guard lines, the relays RG

and SG are not energized. But if, through error, two or more runner or stake signals are imposed on the guard lines (from, e.g., other runner or stake cells), the relay RG or SG will be energized, and, there being a direct wire connection — not shown — from the left side of each guard relay to the runner and stake lock relays RL and SL at left, they are energized, and that sets remedial action in train.]

Then (for example) the runner guard relay (RG) senses a dual runner signal, it energizes runner lock relay RL, closing contacts RG1 and RL1 and latching the relay at key RLK (which is released only by manual operation); the runner guard (orange) signal proceeds then to energize hold-up relay HU. That action pulls open contact HU4 and the LM solenoid is de-energized, setting the commutator-scanner bar in rapid rotation. Because the hold up circuitry keeps the contacts HU4 and HU5 open, the solenoid LM cannot be energized and the scanner does not respond to TIM bid signals (brown), and the "connect" signal (purple) CN terminates. A visible alarm-light RGL turns on. No ACK (green) signal returns to the TIM, the relay TC does not operate, and, in consequence, the latch on cam TCC does not lift, and control cam CMC rotates only to move the guide from the cam highpoint

into the cam groove, opening contact CM2 and drawing it down to its lower, ground contact, grounding the connect (purple) signal line. A consequence is that TIM alarm lamp (TL), above and to left of the commutater, is lighted. The TIM is, in effect, locked up. The two alarm lights RGL and TL advise the maintenance staff of the kind of problem involved and of the TIM involved. If the difficulty is local to the TIM, that TIM can be taken out of service by manual operation of the TIK switch (seen just left of the lamp TL), and the data processor restored to service by manual operation of the runner lock key RLK; that key opens contact RL1 and deactivates the holdup circuit (HU), permitting the scanner and the other parts of the system to resume operation. If there is some other correctible fault, not disabling the TIM, then, after correction, the "cancel fault key" CFK, to the right of the three cams, is manually pressed down with the effect of closing contact CM1 and routing an activating signal which operates the cancel solenoid; that solenoid releases the latch holding the control cam CMC in arrest; rotation of cam CMC resets the TIM for resumed sales.

The functional or block diagram of Handley No. 2,479,681, in the record as Ex-

hibit BS, is a convenience in reading Handley against the claims of plaintiff's patent [Tr. 2914-2925 (claim 20) 2925-2928 (claim 21), 2928-2932 (claim 22), 2937-2943 (claim 23), 2943-2951 (claim 24), 2951 (claim 25), 2951-2958 (claim 26), 2958 (claim 27), 3170-3264 (cross-examination)]. Much here depends on what the fair embrace of the claims is.

It can be said at once that claim 20, in the light of Handley's circuitry as just described, as seen in Exhibit BQII, and as summarized in Exhibit BS, can be read on Handley No. 2,479,681 with two qualifications. The first of these is the presence in claim element 20(B) of the phase "representing the particular" TIM, in referring to the signals generated in response to the "selected-transaction" signal. The meaning of the phase, read against the Weida patent's disclosure (easiest seen in Annexes A and E), is at best uncertain, and, in any event, as used in Claim 20(B) relates only to the signals, not to any use made of the two fold nature of the signals (See Exhibit 11, 11A); the bid (brown), contact (purple), runner (blue) and stake (yellow) chain of signals does identify the TIM necessarily, although the identification is not used in any aggregation process. The second qualification is with reference to the null phrase at the end of claim element 20(C) "only if the transaction

is correct." As explained above (pp.174-175) no content can be given to that phrase.

That Handley is essentially electromechanical and not an electronic digital processing system does not distinguish it. Plaintiff's patent is not on a new, unobviously new means of substituting EDP components in familiar racetrack circuitry. It does not limit its claims to EDP components. The patent claims in issue are systems claims, each consisting in a combination of inclusively indicated means that consist in reality of circuitry connecting conventional elements for conventional uses, the whole enacting an old scenario. The union of means claimed by Claim 20 is an unimaginative joining of the basic means of any aggregator of TIM data, means of picking up the wagers (or sales, or whatever the machines handle), adding them by classes (or performing some other calculation on them), and acknowledging (confirming) to the source that the calculation has been made. Handley does these things. His class aggregators are typified by the "1 and 2 combination counter" 39 and the total aggregator by the "total counter or register" 40.

Claim 21 elaborates claim element 20(C), and includes claim elements 21(C) and 21(E), which refer to the reading-in and reading-out steps specific to a counting means that has to retrieve a number, increment it in a separate procedure and restore it to its "address." These elements are not present in Handley, which uses electromagnetic adders. If the claim is pointedly intended to be limited to a "memory" and "updater" aggregating means, it does not read on Handley. But so limited, the claim is empty of any vestige of patentable novelty. The Claim then adds nothing to Claim 20 except to put forward the idea that a "memory" and "updater" could be used as the means of element 20(C), which is self evident. Claim elements 21(A) through 21(B) are then seen as a single "means," specifying the use of an addressed memory and updater type of adder, and the Claim is reduced to nothing.

Claim 22, if read as requiring a register in one central place of the number of transactions at each TIM, and that the register be of the "memory" and "updater" type, does not read on Handley. Handley's register of the number of transactions is kept by stake classification at the TIM in the assembly called "cash counters." See Handley No. 2,479,681, Col. 1, lines 50-60, and cannot be derived from the runner and total

aggregators. For reasons already explained, Claim 22 is of no moment.

Claim 23, relating to scratches, reads on Handley. True, Handley simply and directly picks off the forbidden signal at the "cancel relay" and uses it to close relay A or B and despatch the reject signal to the TIM. But to argue that Handley's is not a species of "comparing" means within claim element 23(C) is to reduce that claim to nothing; a "comparing means" in the strict sense of "a conventional equality comparator" (Exhibit 1, Col. 14, lines 35-36) serves no purpose except to determine that the signal is or is not wanted and to reject the mistaken signal; a glance at Figure 2 of the patent at once suggests that Handley's means are a full equivalent of the comparator of the patent. Hence, reading claim element 23(C) so narrowly as to make the entire claim turn on the precise use of a "comparator" to originate a scratch signal that produces a reject signal rather than a relay pick-off that uses the signal to energize a second relay to produce a reject signal narrows the entire claim to a trivial specificity which denies any originality to the claim as whole. As pointed out earlier, no patentably new union of means is present in the claim, but the constriction of claim element 23(C) in an ef-

fort to save the claim from the challenge of complete anticipation trivializes the claim and reveals its want of patentable novelty in the strongest light. The argument that Handley does not anticipate because of the mutual exclusiveness of function in relays AC and RC in the acknowledgement circuitry, and the consequent risk of erroneous ticket issue, does not reach the point of the present claim. The acknowledgement circuitry of Handley is not assured against certain conceivable errors, but it is a straightforward acknowledgement means operable in the generality of instances, and it fully responds to claim element 23(E).

Claims 24 and 25 relates to scanning means and means for stepping to the next TIM both when no wager is sensed, and after processing the wager when a wager signal has been sensed. Handley does provide scanning means of the required kind unless the scanning means must generate a TIM number, and unless Handley's non-stopping scan ignores sensed wager signals. But the claims do not in terms or in reason require that the scanning generate a TIM number. They require simply that the scan proceed from TIM to TIM for interrogation. Indeed, since the scan signal that reaches the TIMs of plaintiff's patent has been decoded by the scanner, it may be questioned whether its probable derivation

from a TIM number signal has any functional relevance or significance at all in the ultimate interrogation of the TIM. Nor does the rotation of the scanning bar and its slowing (rather than stopping) at the active TIM under the influence of the LM solenoid result in a failure to "step" only when appropriate. The peripheral dimensions of the segments allotted to the TIMs and the speed control would, as of course, be measured to allow for a brush-contact time sufficient for the processing of any sensed transaction.

Claims 26 and 27 relate to aspects of the "error test routine" of plaintiff's patent. Exhibits 16, 16A and the testimony of the patentee Weida appear to confine plaintiff's view of Claims 26 and 27 to the functions centering on the "two entry transaction" unit THBA ("a conventional majority logical element") as distinguished from the means of detecting attempted wagers on scratched horses, centering on the "test for non-transaction" unit TFSA; Claim 26 is treated as including acknowledgement means where the wager is valid and rejection circuitry for the case in which erroneous entries are sensed. Claim 27 is treated as specifying the test for the attempted dual wager. The use of the plural "signals" in claim element 26(B) in contrast to the

pointed use of the singular "signal" in claim element 26(A)(1) and 26(C) lends support to that reading.

The dual entry circuits (orange) of Handley respond to Claim 27 and claim element 26(B) in displaying means of detecting and acting upon dual entry and stake signals. Strictly, the operation of the Handley circuit locks out the TIM rather than simply rejects the transaction, and the TIM must be restored to action through operation of the cancel fault key. Where there is no dual entry, Handley does transmit an acknowledgement signal. The argument that the acknowledgement signal would arrive before the lockout system could function has no support except in a comparison of the number of relays in the error circuit with the number in the acknowledgement circuit, but operating times of relays differ and the times are not given in Handley's specification.

The detailed consideration of Handley demonstrates the overall absence of patentable novelty in the patent in suit. It brings out sharply the extent to which familiar circuits have long handled familiar tasks, and that the plaintiff's patentees brought no new discovery to the task but only a routine choice of familiar but newer means to

replace the older ones of Handley in the same union of means. The union embraced in each claim Handley shows to be itself old, the asserted differences between Handley and the plaintiff's patent that plaintiff relies on, emphasizing differences in the means and not in the combinations or unions of means that, broadly, were equivalents, underline the want of novelty in the union of means — the combinations, on the patentable novelty of which validity absolutely depends.

The Aqueduct Totalizator System of 1960-1961, discussed by the witness Fosse in detail (see particularly, Tr. 1939-1954) and summarily by the witness Highleyman (Tr. 2959-2965), is most easily seen in Exhibits X and BT, and it is illustrated in terms of typical operating subsystems and components in Exhibit AA. It does not duplicate Handley, but like Handley exhibits unions of means embracing, as of course, TIMs, individual runner and total aggregators, scratch horse wager rejection means usable to detect and reject an effort to aggregate wagers on two runners on the same scan, scanning means, and acknowledgement means. The Aqueduct totalizator did not have means to record the number of bets placed at each TIM and, thus, could not be

said to respond to Claim 22. Like Handley, it does not exhibit claim elements 21(C) and 21(E), but the point of claim elements 21(A) through 21(E) is simply to state "aggregator means," and such means the Aqueduct totalizator possessed, as did Handley. Again, as in the case of Handley, the Aqueduct totalizator illustrates the absence of any novelty in plaintiff's claimed unions of familiar means to perform their usual functions with their usual effect in a simply additive way. That the Aqueduct totalizator is closely related to Lange No. 3,051,384, cited in the Patent Office, does, indeed, signify that the Patent Office granted the patent over Lange, and that, therefore, the patent is entitled to a presumption of validity over Lange. But the presumption evaporates when the patent is scrutinized in the light of Handley (cited in Lange) and the Aqueduct totalizator itself. The facility with which the patent was issued remains inexplicable.

Except that it uses a good many electronic components, it is not suggested that Wright No. 2,837,281 (Exhibit BQ-2) displays as clearly as Handley and the Aqueduct totalizator the defining characteristics of Claims 20-27 of plaintiff's patent, in some part, it would seem, because the subject

matter of the patent did not require a total elaboration in the specification of the system involved. Hence the reading of the claims on Wright's disclosure is imperfect, and Wright inures as an additional but more general evidence that the plaintiff's patent does not present patentable novelty or any patentably novel union of means but mere difference without advance. The same must be said of Faulkner No. 2,987,250 (Exhibit BQ-3), an "electronic totalizer" displaying a "sequential" scanner, plural TIMs, runner and totals aggregators with memories" and "updating" means, and acknowledgement means. Reach No. 3,063,036 (Exhibit BQ-4) is dilutedly like Faulkner and of the same species as Schrimpf (Exhibit 3A), which was so inadequately dealt with in the Patent Office. The other prior art discussed in posttrial briefs and proposed findings is remoter in terms of claim reading, but all contribute something to the demonstration that plaintiff's patent presents, simply, one modest example of the wealth of suggested means of converting such data processing systems as racetrack parimutuel systems to the use of electronic components without presenting any patentable advance over the existing art or commercially available means of adaptation.

VIII

The issues of infringement have not played a prominent place in the case, in part, no doubt because the seeming breadth of claims 20-27, and plaintiff's reliance on Section 112, third paragraph, left meaning somewhat at large, to roam and pounce. See, e.g., defendant's proposed finding 124 and plaintiff's approach in its proposed findings 8.1 and 8.13. But in the end, defen-defendant means Claim 24) and 128.

A. The argument that the accused devices do not involve periodical and sequential scanning means within the meaning of claim element 24 must fail. The gist of the defense argument is that in the device of the patent a STEP signal from the step pulse generator STP (Fig. 3) (which is started up by console signal ICL) sets the scan counter SKA at one or increments the scan counter SKA (Fig.2) by one, and so causes the scan counter to feed an SKNA signal to scanner SCA, which decodes it and sends it as signal SCNNA to the interface (IFN) of the first (or the next) of the TIMs N. If the TIM has a transaction ready, as manifested by a depressed key and the TIM generation of BID N signal, the signal at the TIM (now SCNN) crosses the switch, closed in

response to the depressing of the TIM key, and "is fed out as a selected transaction signal" HNN to buffer NA, and then is processed. If TIM N is not ready with a transaction, what really occurs is a little obscure (Exhibit 1, Col. 4, lines 40-45), but the specification states that if no transaction switch was "latched the STEP signal was generated. Therefore, this is the method of stepping over [TIMs] which are not prepared to perform a transaction." The SCNNA signal from the scanner SCA is the interrogation signal (Exhibit 1, Col.3, lines 44-45). In any case, plaintiff's scanner presents each TIM in numerical order with the opportunity to connect for service and connects for service with TIMs in their numerical order. Since it sweeps over a large number of TIMs cyclically, it does not take up bids for service in the time order in which the bids for service are put up, but in number sequence by cycles. That is, if TIM 50 gets its bid up before the scan passes it is served when the scan reaches it even though TIM 80's bid may have been made an instant sooner. So too, if the scan is at TIM 50 when TIM 49 puts up its bid, TIM 49 must wait until the scan completes the cycle, serving TIMs all of which may have bid later than TIM 49. The cycles are so frequent that no practical delay is present, the patent assumes.

The accused TIM scanning system common to both accused devices is easiest seen in the sketch, Exhibit BU, of the "NYRA Cascade Scanners." It will be seen that while each TIM scanner scans its group of fifty TIMs "sequentially" in the same sense of that word that applies to plaintiff's scan, and the master scanner scans the TIM scanners "sequentially" in that same sense of the word, the order in which the TIMs are served will be a complex sequence. If a letter is assigned to each TIM to reflect its group, scan will always be, it seems, in the order An, Bx * * * Ly; but, although the numbers will seem random, they will be ordered within each letter group. That is, using groups of six and four letter groups for simplicity, the order could be:

```
A1          2           3           4

B  12,        7           8           9

C     15,         16          17          18

D        20          21          22          23
------------------------------------------------------
   1, 12, 15, 20, 2, 7, 16, 21,  3, 8, 17, 22,  4, 9, 18, 23
A  5        6           1            2

B     10          11          12          7

C        13          14          15          16

D          24          19          20          21
------------------------------------------------------
   5, 10, 13, 24,   6, 11, 14, 19,   1, 12, 15, 20,  2, 7,16,21
```


The sequences shown assume that every TIM is always ready with a bid when reached by its scanner; that is a condition to which the scan system must be equal, but it is not an intrinsically necessary condition. The service sequence is logically the same, although more numerically obscure since there will be skipped numbers, but never skipped bidding numbers, in one or more groups; every TIM ready with a bid will be served within its group in number sequence within the cycle of its TIM, for no scanner is adapted to pass a bid or to relinquish the TIM connection until service is complete, at which point it scans on to the next bid in sequence and initiates service.

Do the accused systems, then, include "scanning means for sequentially and periodically selecting each of the TIMs for interrogation"? Each TIM is scanned sequentially by its scanner and, within each group, bidding TIMs are served sequentially. That a dozen scanners are seeking service at common aggregators so that they too must feed their collected selection signals through another collector in that collector's sequence does not signify that the TIMs have not all been scanned sequentially. It signifies only that the complex ordering of the servicing obscures the sequences of scan and service.

That the scan is never "periodical" in one

sense, since scanner's dwell-time is longer at bidding TIMs than at inactive TIMs, does not mean that the term defeats the claim element and makes infringement impossible. It is periodical in the sense of occurring in a regularly repetitive cyclical pattern that is uninterrupted. The "period" of scan is once every cycle.

B. Defendant strongly urges as its general infringement defense to Claims 20-27 that the reading of the claims on the accused devices depends critically on finding that the general-purpose computers used in the accused systems execute the functions of the "means" of the plaintiff's claim elements through use of stored "programs." Plaintiff, it is contended, seeks to find infringement in defendant's method of using a completely non-infringing general purpose machine. Defendant puts it:

> "Simply stated, the basic issue posed is whether an apparatus claim for combination of old elements (as distinguished from a process claim) can be infringed where the recited elements
>
> exist only in sequenced transitory states through the interaction of sequentially operative software

> "program" instructions with elements of available standardized and multifunctional circuitry, and
>
> do not coexist as physically identifiable entities at any given instant of time."

Plaintiff answers that, without stored programs a general purpose data processor is useless; that a data processor physically stores a program as a physical condition of the processor — the physically stored program endows the data processor as a machine with the capability of functioning in particular ways, converts it into a physical means of performing that function. The general purpose processor, therefore, plaintiff appears to argue, embodies physically, if temporarily, the unions of means of the patent claims in suit; that it can accept many other programs and embody physically many other unions of means that do not infringe, plaintiff appears to argue, is beside the point — infringement need not be the necessary and inevitable effect of every operation of the general purpose computer: it infringes when it physically harbors in its memory cores, flip-flops, etc., the stored signals, magnetic states, etc., which make it an operable assemblage of physical means of performing the set of functions which the system or device of the claim is dedicated to performing. Putting

aside Gottschalk v. Benson, 1972, 409 U.S. 63, 175 USPQ 673 as dealing with a "software" program for solving a mathematical formula on an existing computer, plaintiff invokes Application of Knowlton, C.C.P. A. 1973, 481 F.2d 1357, 1368, 178 USPQ 486, 494, and could invoke Application of Johnston, C.C.P.A. 1974, 502 F.2d 765, 771, 183 USPQ 172, 176-177 in which the Court said:

> "Record-keeping *machine* systems are clearly within the 'technological arts.' Such *machine* systems, which comprise programmed digital computers, are statutory subject matter under the provisions of §101, and 'claims defining them must be judged for patentability in light of the prior art.' "

Certiorari was granted in Johnston on May 12, 1975, sub nom. Dann v. Johnston, 44 L.W. 3042. Application of Bernhart, C.C.P.A. 1969, 417 F.2d 1395, 1400, 163 USPQ 611, 616 relied on in Knowlton and Johnston, had said:

> "* * * if a machine is programmed in a certain new and unobvious way, it is physically different from the machine without the program; its memory

> elements are differently arranged. The fact that these physical changes are invisible to the eye should not tempt us to conclude that the machine has not been changed. If a new machine has not been invented, certainly a 'new and useful improvement' of the unprogrammed machine has been * * *."

Judge Rich, dissenting in Johnston, pointed out that Benson, denying patentability to a novel program as a method, implied that the result would be the same if the claims had been cast in machine form (502 F.2d at 773, 183 USPQ at 178-179).

Defendant attacks the plaintiff's argument with the classic differentiation between machine and process claims, emphasizing that a process is a mode of acting, an act or series of acts. Tilghman v. Proctor, 1881, 102 U.S. 707, 722; Expanded Metal Co. v. Bradford, 1909, 214 U.S. 366, 384 (quoting Cochrane v. Deener, 1877, 94 U.S. 780, 787.) Defendant argues, too, that there cannot be infringement of a product claim on a combination of functional means unless the several means in the thing or things or acts accused of infringement are co-existent things that coact to achieve the union function of the combination of means put forth in the patent claim. Cf. Beecher Mfg. Co. v. Atwater Mfg. Co., 1885, 114

U.S. 523 (claim on "the series of dies" [both old] "for forming clip kingbolts"; the dies were to be used successively, and, when so used, in a heat process, the first gave shape to the bolt wings, and then the second, in a separate step, bent the pre-shaped wings to a desired curve; results separate, dies not combined in one machine, "did not co-operate to one result"; no patentable combination). (Many years ago 1 Robinson, Patents, 1890, §173, p. 257, defined a "machine" as "an artificial organism, governed by a permanent artificial rule of action, receiving crude mechanical force from the motive power, and multiplying, or transforming, or transmitting it, according to the mode established by that rule.")

There is no logical defect in plaintiff's argument, nor is the risk unreal that to yield to plaintiff's argument will confuse process with article inventions and open a new order of difficulties in differentiating process from abstract principle. Cf. Waxham v. Smith, 1935, 294 U.S. 20, 21-22, 24 USPQ 34, 35. Benson, certainly, dealt with what was put as a process claim, but the Court was aware that, "Some of the digits are stored as *components* of the computer." 409 U.S. at 65, 175 USPQ at 674, underlining added. The Court knew it was dealing with a method of

implementing a general-purpose digital computer to perform the task of converting binary-coded decimal numerals into pure binary numerals by installing in and feeding to it a congeries of electric impulses, magnetized spots, and charged spots on cathode-ray tube screens. Yet the Court said (409 U.S. at 71, 175 USPQ at 676), "* * * one may not patent an idea. But in practical effect that would be the result if the formula for converting BCD numerals to pure binary numerals were patented in this case." Noting that the formula was of no utility except for EDP roles, the Court said that to validate the patent would pre-empt the algorithm itself. Nevertheless the Court cautioned that Benson was not to be read as precluding a patent "for any program servicing a computer."

What Benson says does not dispel uncertainty, but it lends enough light to see to the conclusion that a combination of means claim comprising a machine system is not infringed by another machine system which does not as a permanent machine system include the same combination of means, and which performs the function to which the patented combination of means is addressed only when its general-purpose digital computer element is "instructed" — programmed — in the processing of the type of raw data that is to be fed to it. It is not the com-

puter — the machine qua computer — that performs the function, but, rather, the machine function of the patent is attained only through "use" of the general-purpose computer. The general-purpose digital computer is itself a total and self-complete machine entity. Versatility in electronic data processing is its endowment, its reason for being, its stock in trade. When it is programmed to do what the system of plaintiff's product patent is capable of doing by machine means, it is not infringing the machine patent, for the patent is on a specific set of machine means, their making, use or vending; the patentability of the combinations of means for performing, inter alia, the tasks of a racetrack parimutuel system, if they had been patentable, would reside in the unobvious novelty of its combinations of machine means for doing the tasks. The programmed general-purpose digital computer does not so do the racetrack job; it does the same tasks but not by the same or equivalent machine means. Rather, it performs the tasks — putting it most favorably to plaintiff — by a new use of a known machine, and that is a process under 35 U.S.C. 100(b).

It is concluded that the accused devices do not infringe Claims 20-27.

IX

The wholly unsatisfactory processing of the patent application in the Patent Office is compounded by want of total disclosure on the plaintiff's part of the antecedents of the first totalisator and of the patent application. But the evidence does not support a finding that there was conscious wrong-doing or witting non-disclosure of what plaintiff knew or should have known was germane to the prosecution of the application. A too cavalier assumption that plaintiff could farm out to Spiecens the job of preparing a hurried application that could be filed and wrangled out later on in the Patent Office there may have been. There was a chilling disregard of the principle that it is individual human inventorship only that the patent law recognizes and not corporate ownership of technical talent and the technical men's derisory "rights" to file for patents on their inventions. Here, the evidence is that Spiecens dealt with the "inventors" orally, worked from shop drawings, schematics, block diagrams etc., and, evidently, neither felt that he had to, nor did dig into the background. He was filing on the system just completed, and the walkover prosecution did not occasion any return for client conferences that would have

exposed the roots of the system his specification described and his claims outlined. It does not appear that Leonard or Weida or any management personnel withheld anything against Spiecens's inquiry or suppressed anything which Spiecens thought he needed or which management feared might become a threat to successful prosecution. The overall impression is that the filing was not a matter to which management attached any importance or to which it adverted after authorizing the filing. The conscious misdealing with the Patent Office or the reckless neglect of disclosure responsibilities required by the authorities were not present. Cf. Carter-Wallace, Inc. v. Davis-Edwards Pharmacal Corp., 2d Cir. 1971, 443 F.2d 867, 881-883, 169 USPQ 625, 634-637.

It is, therefore, concluded that the patent was not obtained through any fraud on the Patent Office, and, that, although plaintiff's management of the prosecution was characterized by a foolish unconcern, a want of proper managerial and technical supervision, and an improperly broad delegation of responsibility to an inadequately instructed patent solicitor, plaintiff did not act in bad faith in prosecuting the patent as it did, or consciously breach its duty to the Patent Office.

It follows that the case is not within Walker Process Equipment, Inc. v. Food Machinery & Chemical Corp., 1965, 382 U.S. 172, 147 USPQ 404.

There remains the question whether defendants are entitled to reasonable attorneys fees under 35 U.S.C. 285. The case has been pending for about eight years and the trial consumed twenty-five days. Nevertheless it cannot be said that the case was pursued in bad faith, or was so wholly devoid of substance that plaintiff could not fairly be supposed to be proceeding in good faith. Cf. Kahn v. Dynamics Corp. of America, 2d Cir. 1975, 508 F.2d 939, 944, 184 USPQ 260, 263-264. It may be difficult to believe that plaintiff could have thought, or have persuaded its experienced counsel, that the patent reflected any technical or practical advance of any importance. The descent of the case to a hollow reliance on Claim 22 as the most important claim and on claim element 20(B) as a matter of unobvious novelty betrays the slightness of the patent and the tenuousness of the claim that it discloses patentable subject matter. But none of that makes the case one within Section 285. And had the patent and the pendency of the case imposed any substantial constraint on Atusa's trading, the long sleep of the case in the discovery phase, for

the supervision of which the late Judge Rosling had referred it to one of the Court's Magistrates, would not have been suffered to continue.

X

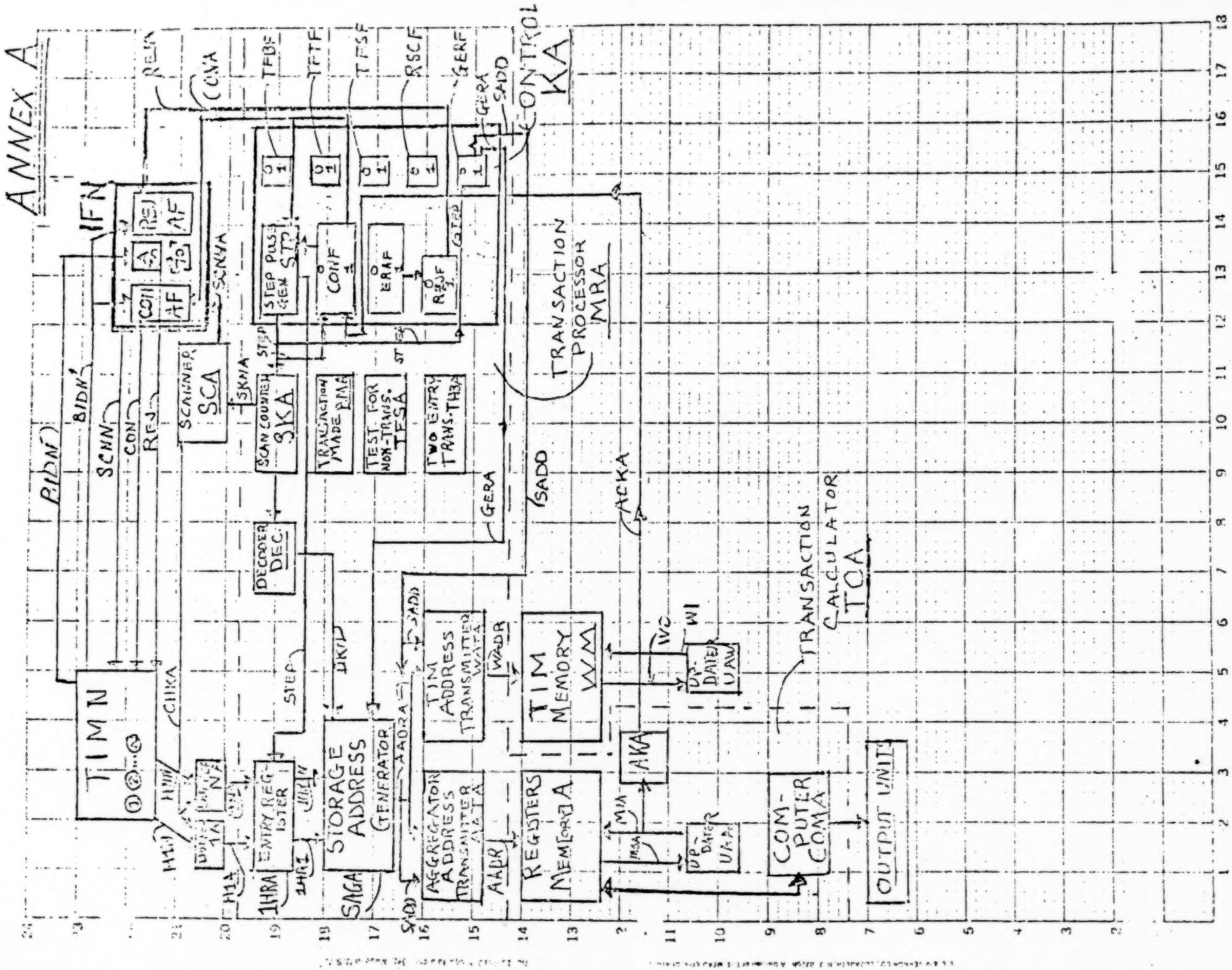
Separate supplemental findings have been made, but the present Memorandum contains the greater part of the findings of fact.

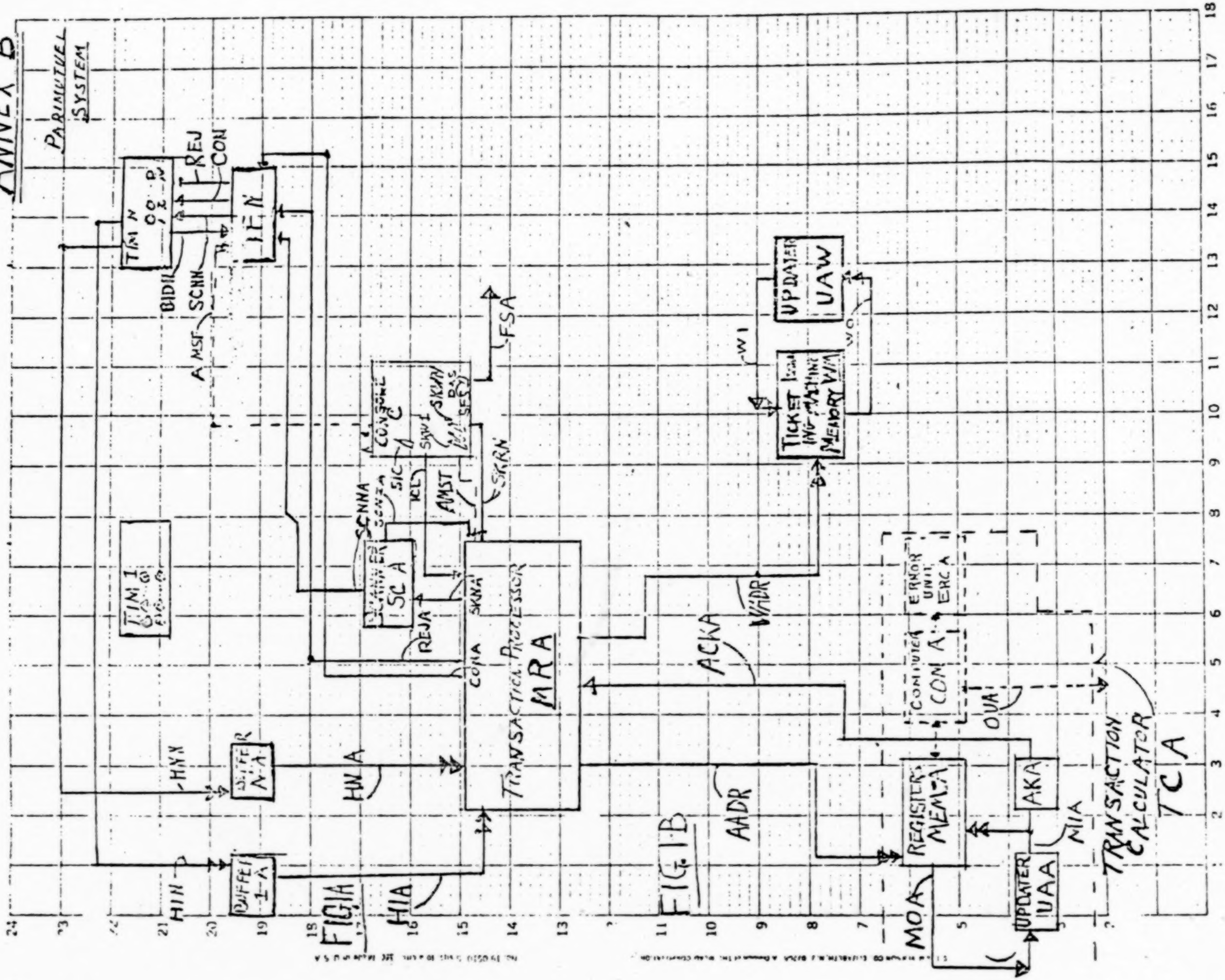
The formal order for judgment is incorporated in the same document with the findings of fact. Judgment is for the defendants.

It is SO ORDERED,

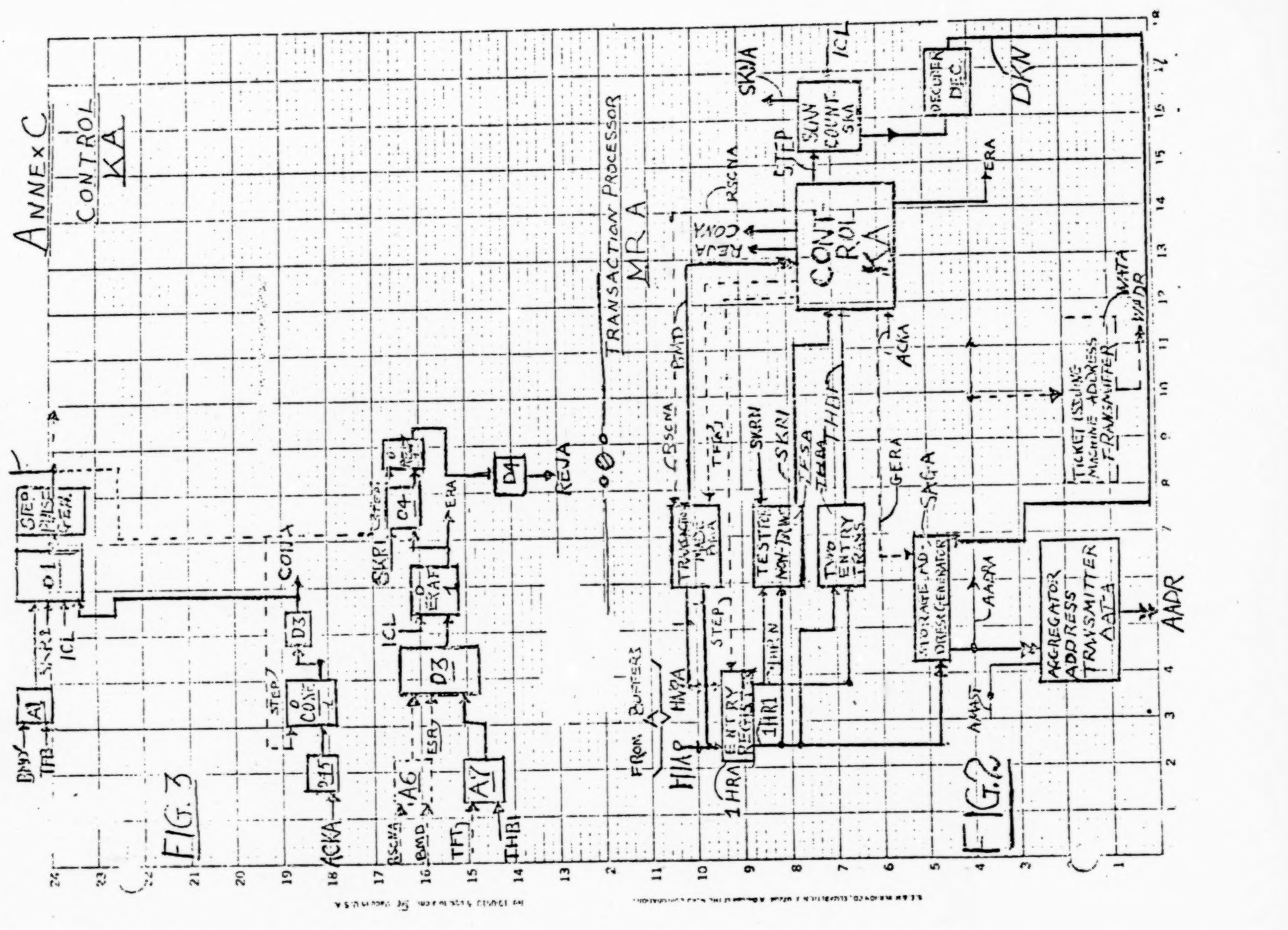
Brooklyn, New York
September 16, 1975

s/ John F. Dooling
U. S. D. J.


ANNEX A
TIMN
SCANNER SCA
DECODER DEC
STORAGE ADDRESS GENERATOR
TIM ADDRESS TRANSMITTER WATA
AGGREGATOR ADDRESS TRANSMITTER AATA
TIM MEMORY WM
REGISTERS MEMORY A
AKA
COM-PUTER COMA
OUTPUT UNITS
TRANSACTION PROCESSOR MRA
TRANSACTION CALCULATOR TCA
CONTROL KA

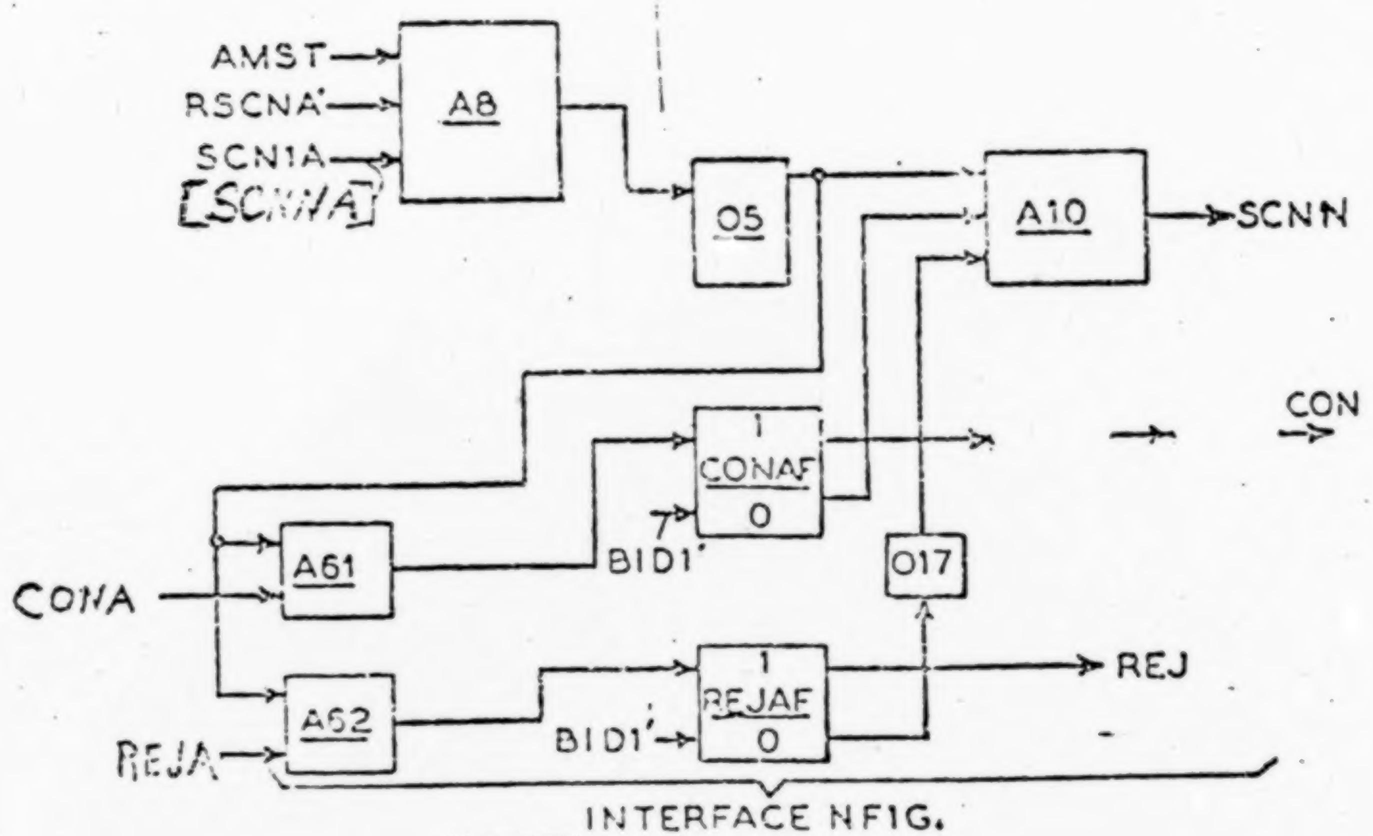


ANNEX B
PARIMUTUEL SYSTEM
FIG 1A
FIG 1B
TRANSACTION PROCESSOR
MRA
TRANSACTION CALCULATOR
TCA
TICKET INFORMATION MEMORY
UPDATER
UAW
UAA
REGISTER MEM A
AKA
CON A
ERCA
SC A
HIA
HWA
AADR
ACKA
WADR
MOA
FSA


ANNEX C
CONTROL KA
TRANSACTION PROCESSOR
MRA
FIG. 3
FIG. 2

At A10, SCNN substitued for SCN1, since single wager, not daily double, involved.

FIG. 4 (See Col 8, ll. 32-43)

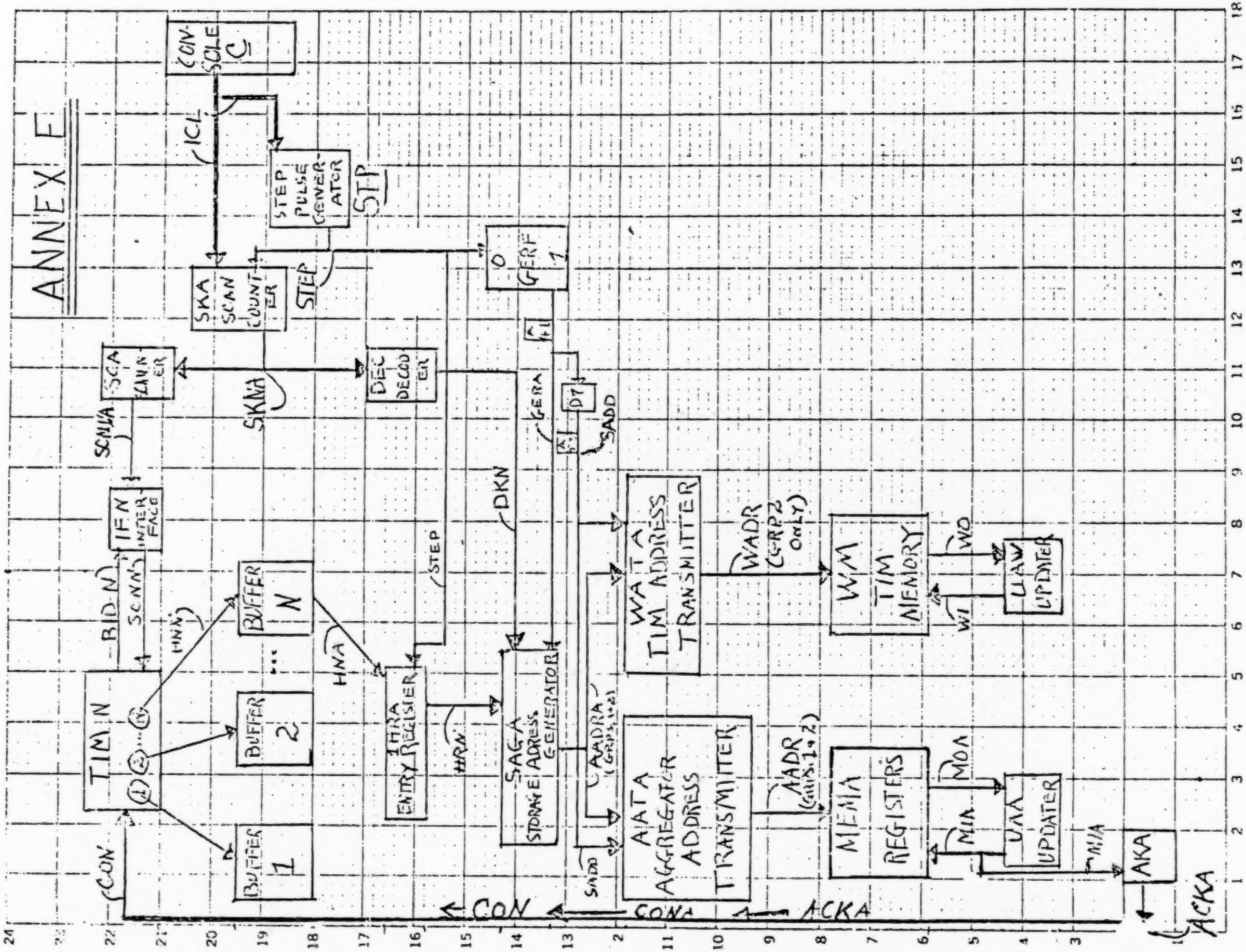


BY

INVENTOR

INTERFACE IFN

ANNEX D


ANNEX E
CON-SOLE C
ICL
STEP PULSE GENERATOR
STP
SKA SCAN COUNTER
STEP
GERF
SCA COUNTER
DEC DECODER
SKNA
SCNNA
GERA
SADD
DT
IFN INTERFACE
BIDN
SCNN
DKN
WATA TIM ADDRESS TRANSMITTER
WADR (GRP2 ONLY)
WM TIM MEMORY
WO
WI
UAW UPDATER
BUFFER N
HNN
HNA
STEP
TIM N
BUFFER 2
IHRA ENTRY REGISTER
HRN
SAGA STORAGE ADRESS GENERATOR
AADRA (GRPS 1+2)
AATA AGGREGATOR ADDRESS TRANSMITTER
AADR (GRPS 1+2)
MEMA REGISTERS
MOA
MIA
UAA UPDATER
AKA
ACKA
CON
CONA
BUFFER 1

ANNEX E

ANNEX F

The language of the specification relating to the plaintiff's Post trial brief argument made at pages 6 - 8 is the following, paraphrased and interpolated only to the extent necessary to make comprehending reading possible.

This invention pertains to data processing systems and more particularly, to systems for processing data received from TIMs.

It is a general object of one aspect of the invention to provide a high speed scanning means for interrogating a plurality of relatively slow operating TIMs for transactions.

Briefly, in accordance with this aspect of the invention, scanning means are provided for sequentially and periodically selecting each of the TIMs for interrogation. Interrogating means transmit an interrogation signal to the selected TIM. If the selected TIM is prepared to make a transaction, it will transmit a selected transaction signal, e.g. HNN, meaning key N has been depressed on TIM N to signify that a better has placed a wager on horse N at TIM N. Means sense for the transmission of the selected transaction signal, which, if not sensed, causes the scanning means (SKA? or ACA?) immediately to step to another TIM for interrogation.

The system includes a plurality of TIMs which accept transactions on entries in a contest. The transactions are operated upon by a data processor (Figure 1A, 1B). The data processor includes a

Console and units such as scanner SCA, buffers 1A, 2A ... NA, a transaction processor MRA and a transaction calculator TCA.

The transaction calculator TCA includes a plurality of registers, a portion of which are aggregator registers, aggregated transaction updating means, a computer, and an acknowledge unit.

A switch in the console C will generate a signal C fed to the transaction processor MRA and the transaction calculator TCA as well as to the interfaces IF1, IF2 ... IFN, so that scanner SCA will control (execute) the sequential and periodic interrogation of the TIMs 1 to N. The transaction processor MRA will process a transaction, that is, check for erroneous transactions and other internally generated errors, and generate storage addresses for the memory positions in the TIM memory whose contents are to be updated and also the addresses of the aggregator registers in the transaction calculator TCA whose contents (the aggregated transactions) are to be updated. The processed transaction information from transaction processor MRA is fed to the transaction calculator TCA which operates on the processed transaction information to calculated odds, pools, payoffs and similar information.

All units are connected by signal lines which transfer signals between the units. Signal lines bear the same reference characters as the signals on the lines, so that when only a signal is mentioned, the signal line is implied, and vice versa. Some signals are shown in a single line for convenience although they are a plurality of lines in a cable. Typical examples are

AADR, WADR, MOA, MIA, and SKNA. The lines shown in the figures indicate only one polarity of the signal such as the BID 1 signal. However, concurrent with this signal line, there are instances where a parallel line carries the opposite polarity of this, such as the BID 1' signal.

By momentarily depressing the initial clear switch SIC on the console, the system is initially cleared (the ICL signal).

The console signal (AMST in dual operation) fed to the interface of each TIM sensitizes these units to interrogating signals such as SCNNA signal from the scanner SCA, and the same signal, fed to the transaction processor MRA, insures that storage address signals are fed from the transaction processor MRA to register MEMA and TIM memory WM. (Emphasis supplied) Similarly, the console signal C is fed to transaction calculator TCA and, more specifically, to computer COMA.

The ICL signal fed to the transaction processor MRA presets the scan counter SKA to its initial count of 1. The output of scan counter SKA is fed as the SKNA signal from transaction processor MRA to scanner SCA. Scanner SCA decodes the signal SKNA and it becomes SCNNA and goes to interface IFN. If TIM N wishes to make a transaction, one of its transaction keys will have been depressed and a BIDN signal will be received by the interface IFN, which has no effect at this time. The scan is now at TIM N for interrogation. The SCNNA signal passes to TIM N as the SCNN signal and it is fed to the common side of all of the transaction-selection switches in TIM N. This signal will pass through to the other

side of whichever selection switch is closed and will be fed out as a selected transaction signal, for example, HNN to the buffer for wagers on horse N, buffer NA. Depressing a key on the TIM causes the closing and latching of the associated transaction-selection switch so that the now transformed SCNNA signal, which has become the HNN signal, is fed to buffer NA and thence to the entry register 1HRA in transaction processor MRA.

At the same time control KA (in MRA, Figs. 2, 3) transmits a test-for-transaction-made signal TFB generated by flip-flop TFBF (Fig. 3) to probe transaction-made unit BMA. If a transaction has been made, as indicated by the presence of a signal such as HNN, a BMD signal is fed back to control KA. If no BMD is fed back, control KA generated a STEP signal to scan counter SKA which steps to the count of n + 1 to initiate the transaction interrogation of TIM N+1. It should be noted that the HNN signal was derived from the SCNNA signal passing through a latched transaction switch and if this switch (or another switch in TIM N) was not latched, the STEP signal would be generated. (Emphasis supplied.) Therefore, this is the method for stepping over TIMs which are not ready with a transaction. The STEP signal, when generated, is fed to scan counter SKA for stepping the scan to the next TIM, that is, TIM N+1. (Column 5, line 16).

After the completion of error test routines (testing to be sure that a bet has been made, that two bets are not being co-signaled, that a scratch is not being bet, and that there is no false signal in the system) the coincidence of the reset

signal, the no bet made signal, and a presently irrelevant signal at "and" unit A5 (Fig.3) sets the GERF flip-flop to 1. The GERA signal which is the output of the GERF flip-flop in its "1" state, strobes the storage address generator SAGA (Fig.2). The storage address generator SAGA is a plurality of "and" units each having one of its inputs connected to the GERA signal line and its other inputs connected to various combinations of one wager signal from entry register 1HRA (i.e., HR1 or HR2 ... or HRN) with a TIM identification signal DK1 or DK2 ... or DKN from decoder DEC, which decodes the signal from scan counter SKA.

The storage address register SAGA, in response to the GERA signal, transmits two groups of signals. (Emphasis supplied.) The first froup, AADRA1 ... AADRAM, is associated with entry transactions (that is, at this part of the specification the "entry" keys are thought of as numbered from 1 to M); the second group of signals AADRAM+1 to AADRAN (signifying numbers of TIMs from 1 to N, apparently) are associated with the TIMs. These two groups of signals are grouped into a cable generalized as an AADRA signal.

After a presently irrelevand disparity check, a delayed GERA signal (Fig.3, unit D7) the SADD signal, is sent to both the aggregator address transmitter AATA and the TIM address transmitter WATA. Both the first and the second groups of the storage address signals AADRA pass through the aggregator address transmitter AATA to become the aggregator AADR signals. The second group of AADRA signals passes through the TIM transmitter WATA to become the memory position address WADR signals.

The aggregator address transmitter AATA is described in Boolean terms at Column 15, line 1 through 20. When the equation is simplified to drop the "B master" possibility, since the claims in suit deal with simplex operation, and the AMST signal, since it too relates to the "A master" operation, comes down simply to saying that the address is transmitted to the memory if the SADD signal is present. This applies equally to the group 1 and group 2 signals, that is, the address identifying the horse or entry on which the wager has been placed and the signal representing the TIM at which the wager was placed. The TIM address transmitter WATA equation, similarly, says simply that the group 2 portion of the signal (indicating that an unspecified wager has been placed at the TIM) goes forward if the SADD signal is present.

In regular, that is, not daily-double wagering, the signal inputs of storage address generator SAGA include only the entry-identifying wagering signal which can be simplified to HR1, HR2 ... HRN signals and the DKN signals (that is, the TIM identification signals which are the output from decoder DEC) both of which will be included in the AADRA signals (Col. 7, lines 72-75). The AADR signal from aggregator address transmitter AATA is fed to register MEMA. The addressing circuitry there receives the aggregator address signals AADR to select the indicated aggregator register. The contents of the selected aggregator address are read out, recirculated and written back into the same selected aggregator register to update the number of transactions. In particular, for example, the AADR signals,

when received by the aggregator register MEMA, select the column assocaited with the TIM and the row associated with the particular entry upon which a transaction is being made. The signals representing the accumulated number of transactions in that aggregator register are read out via MOA signal lines to the updater UAA, where the count they represent is updated by 1, and then is fed back via the MIA lines to the original aggregator register in registers MEMA. At this time, registers MEMA feed an acknowledgement ACKA signal via amplifier AKA, indicating that the transaction has been recorded, to the control KA.

While the entry transaction is being aggregated, the specific TIM transaction is also aggregated. In particular, the WADR signal is fed to ticket issuing machine memory WM. The specific address memory position therein is selected in the manner described above for the register MEMA, and the contents of that address memory position are read out on the WO signal lines and fed via the updater UAW and the WI signal lines back to the same address memory position in the ticket issuing machine memory WM. In this way, a central check is maintained on the number of transactions made by each TIM. For the sake of simplicity, there has been shown only an aggregation of the total transactions made by a ticket issuer. The routine can obviously be refined to indicate also the specific activity on each entry.

The storage address generator SAGA, described in the instance of two entries for simplicity, satisfies two Boolean equations which in the light of Column 7, Lines 74 and 75, can be simplified from

the form of Column 14, Lines 63 and following, so that for the group 1 signals the first expression is

GERA·HR1 = AADRA1
***
***
GERA·HRM = AADRAM.

The second group of signals would respond to the following equations

GERA·DK1 = AADRAM+1
***
***
GERA·DKN = AADRAM+N.

In group two, DK1, DK2 ... DKN imply the different outputs of decoder DEC which decodes the scan counter SKA signal.

It appears that the scan counter SKA is described in terms which indicate that when it is at TIM 1, it is at count 1, when it is at TIM 2, it is at count 2 and when it is at TIM N, it is at count N. When the scan counter SKA reaches a count that is one greater than the number of TIMs, it generates an all-TIMs check signal and then resets to a count of 1. Scan counter SKA is a chain of conventional cascaded binary counters. The scanners SCA and DEC are decoders which decode the combinations of 1's and 0's from the scan counter SKA. Hence the output from the scan counter SKA is identical in time, impulse and information at each "step" when it issues as signal SKNA to the scanner SCA and as an unnamed signal to the decoder DEC. In a word, it is the number of the TIM translated into binary notation.

The registers MEMA are a multiplane magnetic core matrix divided into rows

and columns wherein the core in each plane in the same row and column provides a bit storage for a multibit binary number. A (aggregator registers) is reserved for aggregating transactions. Other registers are reserved to store operation and result information of the computer COMA. Included with the registers are typical row and column selectors as well as read and write amplifiers.

Considering the aggregator registers, each row of matrix associated with the registers may be assigned to a different entry and each column to a different TIM. Therefore, the AADR signal lines are actually a plurality of lines divided into groups. The first group are lines associated with the outputs of the particular entry being made and are coupled respectively to the rows. The second group are a plurality of lines associated with the TIM being processed. Of course, this can be refined so that each column is associated not with a particular TIM but instead with the same category of transaction. For example, in a horse race parimutuel system, one column can be associated with all $2 win bets, another column with all $10 place bets, etc. This is a simple matter since each TIM generally handles only one such type of bet. Under control of a read signal the bits of the number will be read out of the selected aggregator register as signals on the sense windings connected to the MOA signal lines, passed through a means for updating and returned to the same selected aggregator register under control of a write signal. Such recirculation type magnetic core matrices are well known.

The Boolean equation given for the acknowledge signal is essentially meaningless. It simply says that the read-back

number signal after any updating serves also as the acknowledge signal to the TIM.

The TIM memory WM is a similar multiplane magnetic core matrix and associated units, except that its matrix may be considered as having a single row. Of course, it can have many rows each associated with different entries.

It should be noted that the registers MEMA feed data to the computer COMA, which in turn, feeds its result data to the output units of the system. The TIM memory is a dead end. No computations are performed on its stored data and they are not put to the output units. In other words, under the specification, no role is assigned to it except to record the number of wagers played at that TIM.

The summary of the specification speaks of the data processor as comprising, <u>inter alia</u>: a scanning means under the control of step signals comprising (a) interrogating means for interrogating sequentially and periodically each TIM to determine if it is to perform a transaction as indicated by a latched transaction-selection switch and (b) transmitting means for transmitting to the latched switch of a TIM an interrogating signal from the scanning means; a plurality of buffer means each having (a) one input line connected to one of the associated output lines of each TIM, and (b) one output line for transmitting a particular transaction signal indicating that a transaction is desired on a particular one of the entries; sundry error checking and synchronizing means, not presently relevant; <u>generating means for generating storage address signals representing the entry associated with the</u>

particular transaction signal and representing the particular TIM under interrogation; transferring means for transferring such storage address signals as aggregator address signals; acknowledgement signal transmitting means for transmitting an acknowledgement signal to the interrogated TIM with the latched switch for issuing a ticket; a TIM memory comprising (a) a plurality of addressed memory positions each storing the number of transactions made by a TIM, (b) address-selection means for receiving the portion of the storage address signals generated by the transaction processing means for selecting the particular memory position associated with the TIM being interrogated, (c) reading means for reading out the contents of the selected memory position, (d) updating means for updating the read-out contents, and (e) returning means for returning the updated contents to the selected memory position; concurrently operating transaction calculating means comprising (a) register means having (i) addressed aggregation registers for storing the aggregation of transactions processed by the transaction processing means, and (ii) other registers for storing operation and result information, (b) means responsive to the storage address signals generated by said generating means for selecting the addressed aggregation registers represented by the storage address signals, (c) means for reading out the contents of said selected addressed aggregation register, (d) means for updating the contents of said selected addressed aggregation register, (e) means for returning said updated contents to said selected addressed aggregation register, and (f) means for generating an acknowledgement signal which is transferred

to the acknowledgement signal responsive means of the interrogated TIM when said updated contents are returned to said selected addressed aggregator register. The "said generating means" referred to in discussing the register MEMA appears to refer back to the "generating means for generating storage address signals representing the entry associated with the particular transaction signal and representing the particular TIM under interrogation."

FINDINGS OF FACT
and
ORDER FOR JUDGMENT

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF NEW YORK
-----------------------------------X
DIGITRONICS CORPORATION, NOW
AMPEREX ELECTRONIC CORPORATION,

Plaintiff,

-against- 67 C 1119

THE NEW YORK RACING ASSOCIATION,
INC., AUTOMATIC TOTALISATORS (U.S.A.)
LTD., AUTOMATIC TOTALISATORS LTD.
and PREMIER EQUIPMENT PROPRIETARY
LTD.,

Defendants.
-----------------------------------X

The following facts are found, in supplementation of those in the Memorandum and Order:

1. This Court has jurisdiction over the subject matter and parties.

2. Plaintiff, Digitronics Corporation, is a corporation of the State of Delaware. Plaintiff, Amperex Electronic Corporation, is a wholly owned subsidiary of North American Philips Corporation and is Digitronics's successor in interest.

3. Defendant, New York Racing Association, Inc., (hereinafter "NYRA") is a corporation of the State of New York and has a regular established place of business within the Eastern District of New York.

4. Defendant, Automatic Totalisators (U.S.A.) Ltd., is a corporation of New South Wales, Australia, and is a wholly owned subsidiary of defendant Automatic Totalisators Ltd.

5. Defendant, Automatic Totalisators Ltd., is a corporation of New South Wales, Australia.

6. Defendant Premier Equipment Proprietary Ltd. is a corporation of New South Wales, Australia, having a regular and established place of business within the Eastern District of New York and is a wholly owned subsidiary of defendant Automatic Totalisators Ltd. Defendants other than NYRA, united in interest, are hereafter referred to as Atusa.

7. U.S. Patent No. 3,252,149 in suit was issued to plaintiff Digitronics Corporation on May 17, 1966 as assignee of the named inventors Robert L. Weida, Edward M. Richards, Evelyn Berezin, Jack Knoll and Philip Rosenblatt thereof.

8. The application for the Weida et al. patent was filed March 28, 1963. The critical statutory bar date under 35 U.S.C. 102(b) is, therefore, March 28, 1962 (i.e., date invention was patented or described in a printed publication in this or a foreign country or in public use or sale in this country).

9. Claims 1-19, and 28-33 of U.S. Patent No.3,252,149 have not been infringed by defendants, it was admitted at the commencement of trial, and they are not in issue.

10. The validity and infringement of "systems" claims 20 through 27 are here in issue; no evidence was presented to support or challenge the validity of any other claims.

11. Plaintiff conceded that claim 20 is the "heart" of the patented totalisator system and is the dominating claim.

12. Claim 22 is put forward by plaintiff as the most important claim; plaintiff puts forward as useful and unobviously novel the alleged combination of TIM number signal generation, TIM memory and electronic digital means.

13. Parimutuel betting is a system of wagering for multi-entrant events, such as horse racing. The wagers on each entrant for each "place" ("win," "place," "show") are accumulated in separate pools; the betting odds and consequent payoffs on the entrants that "place" (run first, second or third) are determined by the ratios of the total amounts wagered on each of the "placing" entrants to the total amounts (less tax and track's percentage) wagered on all the entrants for that "place."

14. Parimutuel "totalisators," whether manual, mechanical, electromechanical or electronic, are data processing systems.

15. The term "totalisator" connotes a system for automatically totalling bets entered on key-operated ticket issuing machines (TIMs) on runners in a race in order to account for the wagers, and compute payoffs and other betting results promptly after the announcement of the race result.

16. Atusa was early in the totalisator field, claims credit for coining the word and claims a large share in the development of totalisators since the first mechical ticketing device. Atusa developed a practical mechanical totalisator ("tote"), which was put into use in 1917, an electromechanical totalisator in 1917, a multiple pool tote in 1923 and an automatic odds tote in 1927.

17. Totalisator systems for automatically performing the necessary accumulation of individual wagers on the entries, accumulating the total amounts wagered on all entries and making the necessary related calculations for parimutuel betting operations have been in use in this country since as early as 1933.

18. Atusa's first installation in this country was at Hialeah in 1932; a year later that

system was sold to a group which later formed the American Totalisator Company (AmTote).

19. In 1933, AmTote installed at Arlington Park, Chicago a totalisator with a public display of the betting figures which were accurate to the dollar.

20. Over the years AmTote personnel have received and assigned to AmTote, or it has otherwise acquired, patents on totalisators, including

A. No. 2,182,875 on a totalizing system including a stepping switch collector or scanner which operates only on TIM signal;

B. No. 2,179,698 on an electromechanical totalizing system featuring a "jumping jack" collector or scanner; and

C. No. 2,557,384 on a mixed electromechanical and electronic totalizer using a vacuum tube decade (not binary) counter and electromechanical "pulse commutators"; it used stepping "relay" aggregators;

D. No. 2,563,041 on an electromechanical totalizator system with multichannel adding machines;

E. No. 2,652,977 on an analog odds computer for use integrally in an electromechanical totalizator;

F. No.3,051,384 on a totalizator system (Lange, cited in the patent in suit);

G. No. 3,080,114, a further Lange patent on an improved totalizator system.

21. AmTote designed and tested an electronic totalizator around 1945, but it was not rugged or reliable enough to put into practical use.

22. Electronic data processing is inherently many fold faster than electromechanical or mechanical or manual data processing; since transistors and other semi-conductors have become available, electronic data processing components have become extremely compact; no patentable novelty resides in the decision to convert to solid state electronic data processing from one of the slower and larger systems, and to adapt familiar functions and circuits to the use of electronic components is obvious; the economies of time, space, power consumption and related costs resulting from the substitution of electronic components of a data processing system for electromechanical or mechanical systems are attributes of solid state electronics broadly, and do not make obvious modes of using electronic devices in familiar systems patentably new and useful on the basis of the resulting achievement of the familiar economies common to all solid state data

processing systems.

23. The demands of a racetrack parimutuel system on data processing resources are modest: the arithmetic calculations required are rudimentary; the range of input data is narrow, and the data are simple and easily translated into binary terms; no elaborated long-term memory is requisite; programming is simple and direct, and much of it is reducible to permanent wiring of system components; pre-existing electromechanical circuitry readily supplies patterns which are in considerable part directly adaptable to solid state electronic data processing; the service demands on data processing systems of a racetrack parimutuel system present no identifiable difference of technical significance from those of other multiple input situations.

24. The totalisator systems installed and in operation at the Aqueduct and Roosevelt race tracks in 1961 were American Totalisator Model 7J systems. Such systems were essentially electromechanical in nature employing electrical relay circuitry and electrically operable rotary stepper switches. Such systems also included certain electronic data processing adjuncts and were generally representative of conventional American Totalisator construction and mode of operation at that time.

25. The 1961 Aqueduct totalisator system included:

a) about 500 key operable ticket issuing machines of standardized construction,
b) electromechanical aggregators for accumulating the amounts wagered on each entry in a race,
c) electromechanical aggregators for accumulating the total amounts bet on all entries in a race,
d) an electromechanical scanner for connecting ticket issuing machines wanting to place a bet to the aggregators,
e) electrically operable display boards at various locations for the display of entry, odds and payoff information and the like,
f) an "Automatic Observer" for checking accuracy of displayed information,
g) an analog computer for calculating probable odds, and
h) a solid state electronic digital price computer for calculating payoffs, all electrically interconnected to provide for information transfer between components thereof and periodic updating and display of necessary information.

26. The 1961 Aqueduct totalisator system included electronic solid state digital data processing equipment as an operating component thereof.

27. The ticket issuing machines (i.e., TIMs) utilized at Aqueduct in 1961 were of conventional construction and included:

(1) a plurality of selectively actuatable and latching transaction selection switches each associated with a different entry in a race for transmitting a selected transaction signal associated with the selected entry,

(2) an acknowledgement signal responsive means for issuing a ticket having indicia recorded thereon which is related to a latched switch, and

(3) a rejection signal responsive means for unlatching latched switches relating to a scratched entry.

28. The totalisator system utilized at Aqueduct in 1961 included provision for automatically rejecting wagers on scratched horses with accompanying release of latched TIM switches and for checking input data for other errors.

29. The TIMs included in the totalisator system utilized at Aqueduct in 1961 included memory devices for recording the bets made on each entry in each race, pursuant to New York State requirements.

30. Prior to 1960 AmTote serviced approximately 200 racing associations in the United States. By 1962 AmTote had almost a total monopoly of the totalisator business in the United States. Atusa had only a very few installations in this country.

31. AmTote had a very large investment in primarily electromechanical totalisator equipment of the kind it leased for use at Aqueduct and Roosevelt Raceway. It had a long term and continuing interest in using electronic data processing means in parimutuel betting systems, but it had not either built, acquired or acquired a patent on any complete solid state electronic data processing system for parimutuel betting at racetracks before March 1962. AmTote, as late as 1962, was professedly still unconvinced that electronic data processing equipment sufficiently rugged and reliable for racetrack use was available.

32. There was not a long-felt need for electronics to handle parimutuel betting at racetracks; it was evident at all times that introduction of electronic devices ought in theory to make possible savings in time, space, cost, and, perhaps, personnel at racetracks as in other money-handling establishments, and considerable work was

done in designing and, to a certain limited extent in devising data processing components and systems for parimutuel betting at racetracks; however, there was no want of practical, efficient and economically feasible electromechanical and mixed electromechanical and electronic installations in daily use at racetracks all over this and other countries for handling parimutuel betting.

33. By the middle 1950s, an electronic totalisator could have been built that was both reliable and economic.

34. As of 1952, the dual computer-magnetic drum technology was available to build a successful electronic totalisator. By the mid-1950s, transistor circuitry was also available. By the mid-1950s the technology actually used by Digitronics in constructing the electronic totalisator for Westbury was available.

35. AmTote reportedly had an experimental installation at Roosevelt Raceway in 1947 possibly designed along the lines of the Moerman system of his patent No. 2,472,542 (Exhibit 71); the system was used for six weeks to handle the "show" pool and later was junked. A later "Mercury" totalisator installation at Roosevelt, in which about $75,000 was invested, broke down and was abandoned. Both the Moer-

man and Mercury efforts antedated the availability of solid state devices and technology. Other alleged efforts in the 60s, under Swedish auspices and in Canada, are not sufficiently evidenced to warrant any findings.

36. Digitronics Corporation was formed in 1957 by Eugene Leonard, Albert Auerbach and Robert Shaw, all of whom had earlier electronic data processing experience; Digitronics actively sought "systems" business, and, among systems it had supplied was a medical access and analysis system for the Schering Drug Company which involved the electronic scanning of a plurality of lever operable data input stations, the collection and storage of data obtained therefrom on magnetic tape units and the return of selectively generated signals to the data input stations.

37. In early 1959, Digitronics Corporation actively sought, as an item of "systems" business to enhance its corporate income, a contract from Roosevelt Raceway to design and construct a totalisator system employing electronic data processing techniques to replace the electromechanical totalisator system then being employed to handle parimutuel betting at the track.

38. Leonard (of Digitronics) had no doubts or reservations as to Digitronics'

ability to provide an electronic data processing system to perform the requisite totalisator functions for parimutuel betting.

39. Exactly what was comprised in the Demonstrator or prototype is not certainly ascertainable and plaintiff is responsible for that circumstance. In the absence of the plaintiff's production of the evidence that must of necessity have been in its possession and which it has failed to produce defendants are entitled to a finding based on the remaining evidence that:

A. The "Demonstrator" or prototype electronic totalisator system included, prior to March 28, 1962:

a) 16 simulated (non-ticket dispensing) ticket issuing machines and 3 regular (ticket dispensing) ticket issuing machines,
b) electronic solid state aggregators for accumulating the amounts wagered on each entry in a race,
c) electronic solid state aggregators for accumulating the total amounts bet on all entries in a race,
d) an electronic scanner for sequentially connecting the ticket issuing machines wanting to place a bet to the aggregators,

e) an electrically operable digital indicator display board for the display of entry, odds and pay off information and the like,
f) digital solid state computing devices for calculating probable odds and pay offs,
g) an electronic solid state memory for recording the bets made on each ticket issuing machine,

all electrically interconnected to provide for information transfer between components thereof and periodic updating and display of necessary information.

B. The ticket dispensing type of ticket issuing machines employed with the demonstrator electronic totalisator prior to March 28, 1962 included:

(1) a plurality of selectively actuatable and latching transaction selection switches each associated with a different entry in a race for transmitting a selected transaction signal associated with the selected entry,
(2) an acknowledgement signal responsive means for issuing a ticket having indicia recorded thereon that is related to a latched switch, and
(3) a rejection signal responsive means for unlatching latched switches relating to a scratched entry.

40. None of the named inventors of the patent in suit made any conceptual contribution to any of the electronic totalisator subject matter incorporated in the "Demonstrator" electronic totalisator system. The work of the named patentee, Weida, in the three weeks preceding the first start-up of the "Demonstrator" may have embraced (i) correcting a deficiency in the probable odds computation, a matter not claimed in Claims 20-27; (ii) correcting the aggregator so that it did not go from 100 to zero but to 101, which would not involve any conceptual contribution nor is it possible to see how it could involve design change as distinguished from eliminating, within constant design, a limit on the number of binary "places"; and (iii) debugging the system. Such contributions would not constitute the patentee Weida a joint inventor within 35 U.S.C. 116, 256.

41. The Westbury "All Electronic Totalizator" brochure, was published and distributed prior to March 28, 1962; it describes and discloses an electronic solid state totalisator system which includes:

a) a plurality of ticket issuing machines,

b) an electronic solid state aggregator for accumulating the amounts wagered on each entry in the race,

c) an electronic solid state aggregator for accumulating the total amounts bet on all entries in a race,

d) an electronic scanner for sequentially connecting the ticket issuing machines wanting to place a bet to the aggregators,

e) electrically operable display boards at various locations for the display of entry, odds and pay off information and the like,

f) an electronic solid state digital computer for calculating the odds, and

g) an electronic solid state digital computer for calculating pay offs,

all electrically interconnected to provide for information transfer between components thereof and periodic updating and display of necessary information.

42. The Westbury "All Electronic Totalizator" brochure, as published and distributed prior to March 28, 1962, describes and discloses an electronic solid state totalisator system which includes:

a) provision for handling of bets on scratched horses including prevention of issuance of a ticket thereon,

b) error checking of input data and internal error checking within the computer components,
c) duplication of system components and operations performed,
d) provision for handling of daily double betting, and
e) provision for elaborate permanent record print-out for accounting and record keeping purposes.

43. The Demonstrator or prototype included all of the subject matter recited in Claims 20, 21 and 22 (Tr.1814-1823, 3728 et seq.); Claims 20 - 22 read on the Demonstrator-prototype; the contention that the Demonstrator-prototype did not exhibit a plurality of TIMs is unsubstantial; (i) the demonstrator indicated a plurality of TIMs as a critical component of any such system and used illustrative TIMs and TIM dummies to demonstrate the plurality element; and (ii) so far as Claims 20-22 are concerned the plurality of the TIMs is irrelevant to the substance of the claims, which deal with the combinations of elements relevant to processing transactions at any one TIM.

44. Nothing in the specification or claims of the patent limits the claimed inventions to

solid state electronic data processing; in light of the explicit omission of reference to electronic means and components (except in the reference to electronic scanning (Column 10, lines 72 et seq.); contrast Weida patents Nos. 2,848,532 and 3,042,902, Exhibits P and Q, prosecuted by the same attorney of record as the present patent) the claims cannot be read as solid state digital electronic data processing system claims, but must be interpreted as intended to and in form claiming any means embraced in the disclosure of the specification, including any electromechanical or mechanical means that were adequate to function as the indicated means and within the designation of the means language.

45. Plaintiff did not advise the Patent Office of its developmental and attempted commercial exploitation activities relating to and based on the demonstrator prototype and its successful demonstrations that preceded the filing of the application for the patent in suit including:

(a) the Leonard specification and the January 31, 1961 totalisator agreement, Exhibit AP;
(b) the existence, demonstration and nature of the "demonstrator" - prototype electronic totalisator system; the contract of January 31,

1961 affecting it; and nature and extent of Shaw's and Kielsohn's work on the demonstrator;

(c) the distribution of the Westbury "All Electronic Totalizator" brochure;

(d) the contract for the sale of the "First Totalisator";

(e) the nature of the electromechanical totalisator system and electronic adjuncts thereto as employed at the Roosevelt and Aqueduct tracks in 1961.

46. Claims 20 through 27 are invalid for want of patentable novelty in light of the prior art and the requirements of 35 U.S.C. 103.

47. None of Claims 20-27 can be found to be valid over the demonstrator-prototype in light of plaintiff's failure to make disclosure of the details of the device or adequately to explain its inability to do so.

48. The accused devices do not infringe any of Claims 20 through 27 for the reason that such claims do not extend to systems achieving the same functions as the patent's several combinations of machine means claims by using a general-purpose digital electronic data processor with programmed instructions.

49. The evidence does not support a finding that the patentees and Spiecens consciously participated in the execution of a false oath and in filing it in the Patent Office on March 28, 1963. The patentees were not, however, in fact the inventors of the whole subject matter on which patent claims were sought in light of the extent of anticipation of certain claims of the patent by the demonstrator-prototype with which not even the patentee Weida had such a connection as to constitute him a co-inventor of the demonstrator-prototype. The conception of the demonstrator-prototype was not shared by Weida, and its reduction to practice in the successful demonstrator-prototype was completed without any creative contribution on Weida's part.

50. It is concluded that as a matter of law-

A. Claims 20-27 of patent No. 3,252,149 are invalid under 35 U.S.C. 102 and 103; and

B. The accused devices, the NYRA totalisator system and the PDP-8 totalisator system, do not infringe any of claims 20-27.

51. Issuance of the patent was not procured through fraud or concealment or culpable non-disclosure.

52. No violation by plaintiff of the antitrust laws has been shown.

It is, accordingly, Ordered that the Clerk enter judgment,

1. That plaintiff take nothing and that the action is dismissed on the merits with costs as taxed by the Clerk;

2. That claims 20-27 inclusive of U.S. Patent No. 3,252,149 are invalid and have not been infringed by defendants, and

3. That defendant Automatic Totalisators (U.S.A.) Ltd. takes nothing on its second counterclaim and that it is dismissed on the merits without costs.

Brooklyn, New York
September 16, 1975

s/John F. Dooling
U.S.D.J.

JUDGMENT

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF NEW YORK
- -X

DIGITRONICS CORPORATION, Now
AMPEREX ELECTRONIC CORPORATION,

Plaintiff,

-against- 67 C 1119

THE NEW YORK RACING ASSOCIATION, INC., AUTOMATIC TOTALISATORS (U.S.A.) LTD., AUTOMATIC TOTALISATORS LTD. and PREMIER EQUIPMENT PROPRIETARY LTD.,

Defendants.
- -X

A memorandum and order and findings of fact and order for judgment of the Honorable John F. Dooling, Jr., United States District Judge, having been filed on September 16, 1975, concluding as a matter of law, that claims 20-27 of patent No. 3,252,149 are invalid under 35 U.S.C. 102 and 103; and that the accused devices, the New York Racing Association totalisator system and the PDP-8 totalisator system do not infringe any of claims 20-27, and directing the Clerk to enter judgment, that plaintiff take nothing and that the action is dismissed on the merits with costs as taxed by the Clerk; and that claims 20-27 inclusive of Patent No. 3,252,149 are invalid and have not been infringed by the defendants; and that defendant Automatic Totalisators (U.S.A.) Ltd. takes nothing on its second counterclaim and that it is dismissed on the merits without costs, it is

ORDERED and ADJUDGED that the plaintiff take nothing and that the action is dismissed on the merits with costs as taxed by the Clerk; and it is further

ORDERED and ADJUDGED that claims 20-27 inclusive of U.S. Patent No. 3,252,149 are invalid and have not been infringed by the defendants, and it is further

ORDERED and ADJUDGED that the second counterclaim of defendant Automatic Totalisators (U.S.A.) Ltd. is dismissed on the merits without costs and that the defendant Automatic Totalisators (U.S.A.) Ltd. take nothing on that counterclaim.

Dated: Brooklyn, New York
September 19, 1975

s/ Louis Orgel
Clerk

Approved:

John F. Dooling, Jr.
U.S.D.J.

FILED
In Clerk's Office
U.S. District Court
E.D. N.Y.
September 22, 1975

MEMORANDUM
and
ORDER

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF NEW YORK
--------------------------------X
DIGITRONICS CORPORATION, NOW
AMPEREX ELECTRONIC CORPORATION,

Plaintiff,

-against- 67 C 1119

THE NEW YORK RACING ASSOCIATION,
INC., AUTOMATIC TOTALISATORS
(U.S.A.) LTD., AUTOMATIC
TOTALISATORS LTD. and PREMIER
EQUIPMENT PROPRIETARY LTD.,

Defendants.
--------------------------------X

The motions of both parties are in all respects denied.

(1) Plaintiff's motion amend the findings under Rule 52(b) would amount to accepting plaintiff's view of aspects of the evidence in the teeth of the total effect of the trial evidence. The data and arguments now brought forward explain nothing, and could not reasonably be expected to support the suggested altered findings. The theoretical points made rehash what has been carefully decided. If the decision is wrong, repetition of argument rejected in this Court is better addressed to an appellate tribunal.

The affidavits submitted in support of the application answer themselves; the effort they reflect would have been better

employed if addressed thirteen years ago to advising Spiecens adequately or over eight years ago in deciding whether to sue, or, after suit, to make meaningful to both sides the first stages of discovery, in early 1968, or during the five weeks of trial in 1974-1975, to resolve manifest issues of anticipation; today they serve no purpose except to underline the consequence of early neglect.

(2) Defendants' motion to amend the judgment to declare (a) Claims 20-27 invalid because they were not the invention of the patentees, (b) to invalidate the patent under the sale clause (Section 102(b)), and (c) to award attorneys fees on the ground that the case is exceptional is denied.

(a) The judgment, findings and memorandum, taken together, express all the determinations considered appropriate. The point is that none of the patentees contributed to the Demonstrater or prototype. The article of the patent could not be found, on the evidence, to have been patentable over the Demonstrater, and, on the evidence, the Demonstrater was critical prior art. But that does not signify that what Weida et al. filed on did not have to be processed as the Weida et al. invention against all the relevant prior art, and found good or bad in the light of it. See Memorandum and Order pp. 63 et seq.

(b) Timely Products Corp. v. Arron, 2d Cir. 1975, 523 F.2d 288, does not, as appears from Judge Conner's very precise delineation of the requisites of the "on-sale" finding (523 F.2d at 302), authorize any change in the conclusion reached in the Memorandum and Order, pp. 65-67.

(c) Nor do Timely, supra, and Kramer v. Duralite Company, Inc., 2d Cir. 1975, 514 F.2d 1076, support the conclusion that an award of attorneys fees is warranted in this case. Kramer involved what the Court found to be an utterly false claim that the patentee had chosen the angles that were critical to the inventive novelty of the hinge bracket of the patent. Timely too, was a case of a patentee's calculated concealment of a matter germane to the successful prosecution of the Arron patent. 523 F.2d at 297-298, 305. The findings underlying the conclusion reached in the present case make plain the reasons why neither Kramer nor Timely is applicable here. See Memorandum and Order pp. 213-216.

It is so ORDERED.

Brooklyn, New York
January 13, 1976

s/ John F. Dooling, Jr.
U.S.D.J.

THE PATENT

May 17, 1966 R. L. WEIDA ET AL 3,252,149

DATA PROCESSING SYSTEM

Filed March 28, 1963 5 Sheets-Sheet 1

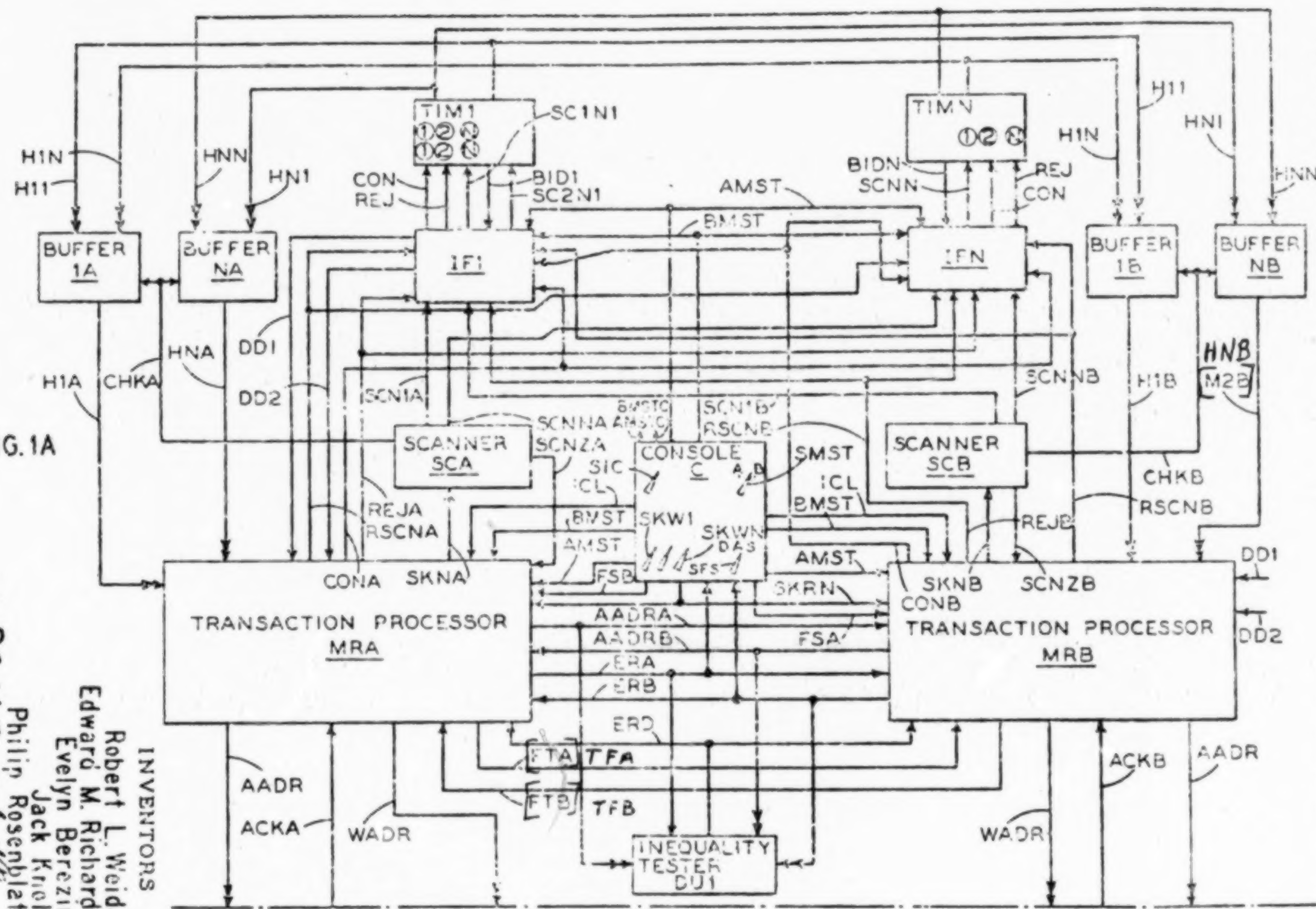


FIG. 1A

INVENTORS
Robert L. Weida
Edward M. Richards
Evelyn Berezin
Jack Knoll
Philip Rosenblatt

BY S.C. Yuter + [signature]

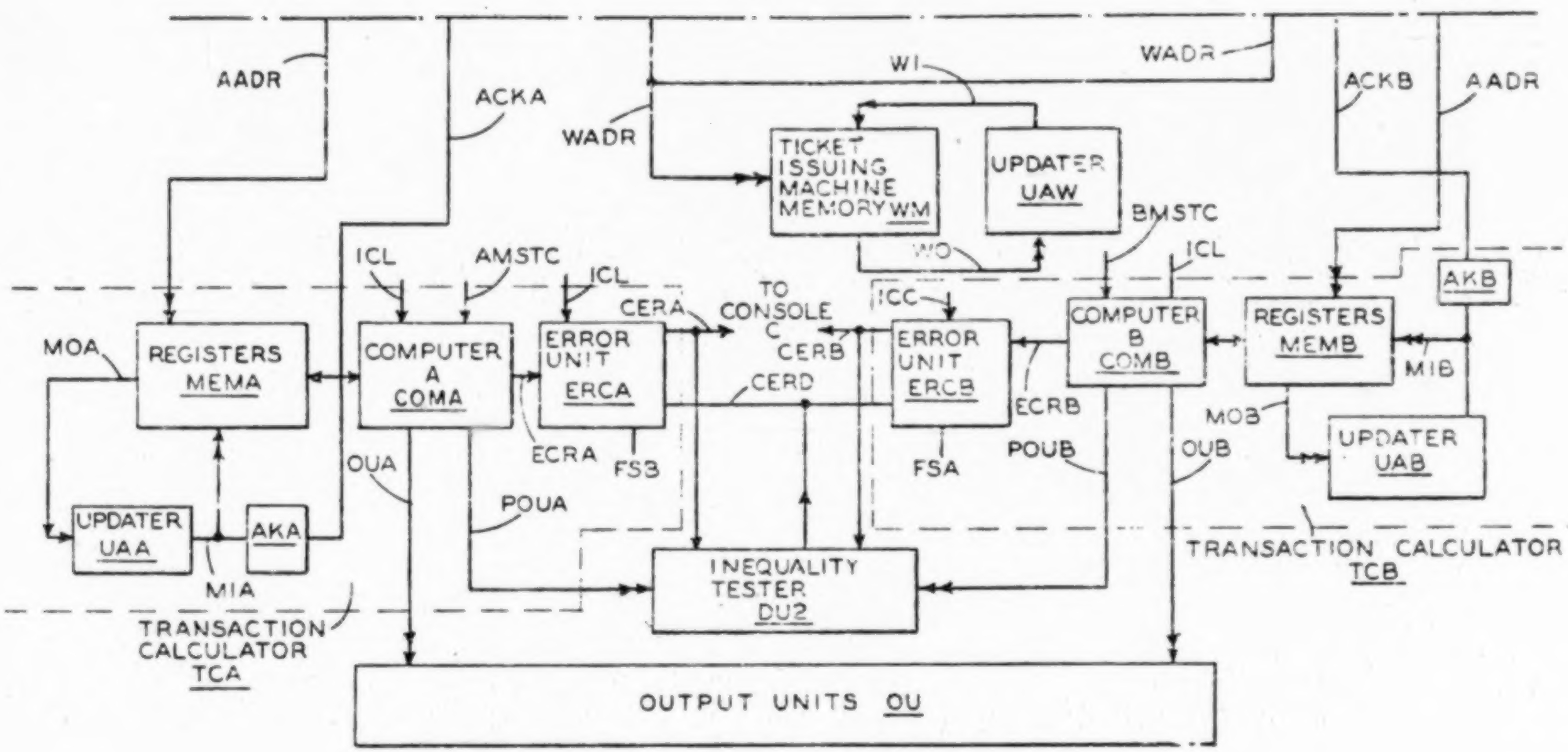
ATTORNEYS

PLAINTIFF'S EXHIBIT 1

67C1119

May 17, 1966 R. L. WEIDA ETAL 3,252,149
Filed March 28, 1963 DATA PROCESSING SYSTEM 5 Sheets-Sheet 2

FIG. 1B



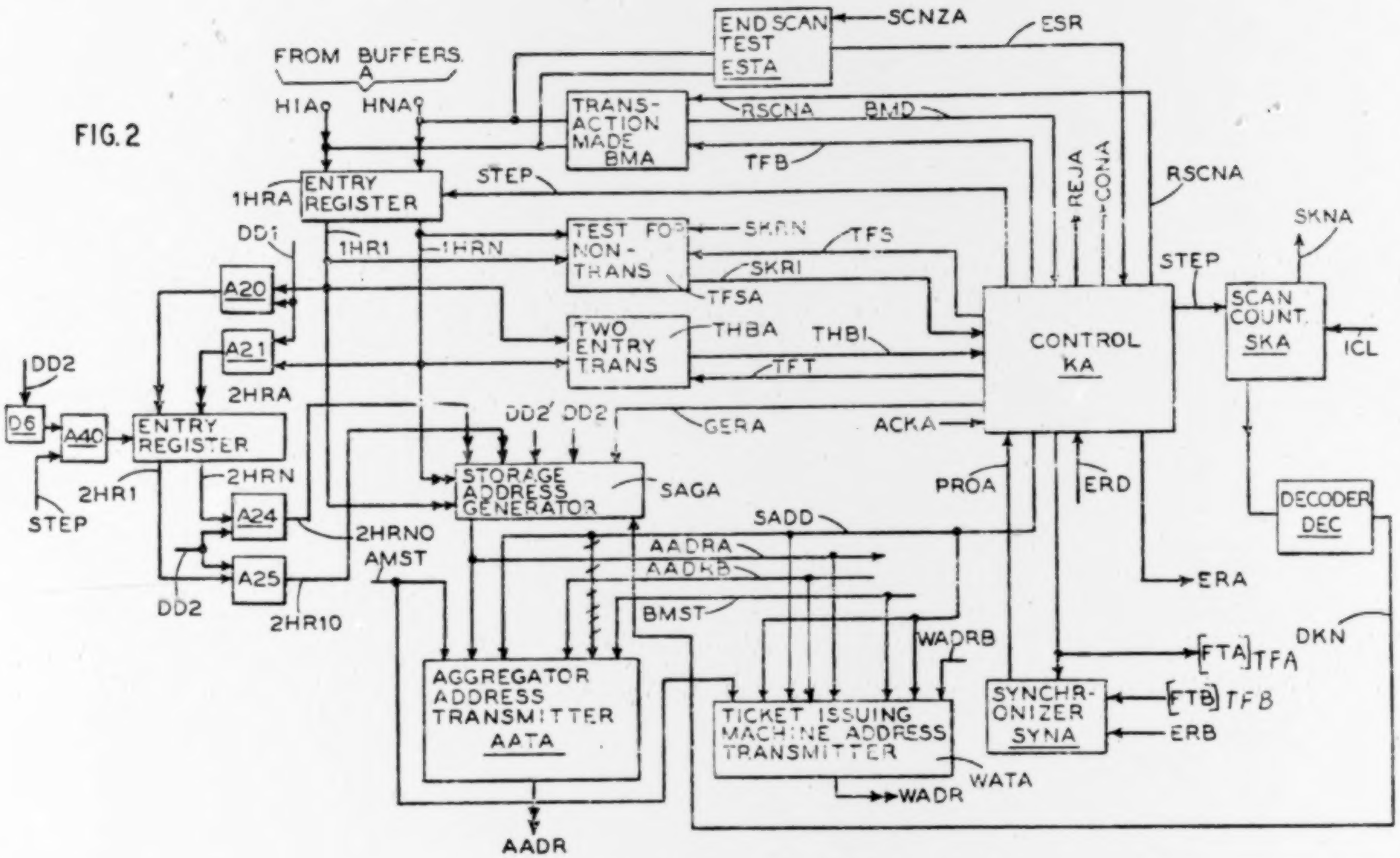
PARIMUTUAL SYSTEM

A263

May 17, 1966 R. L. WEIDA ET AL 3,252,149

Filed March 28, 1963 DATA PROCESSING SYSTEM 5 Sheets-Sheet 3

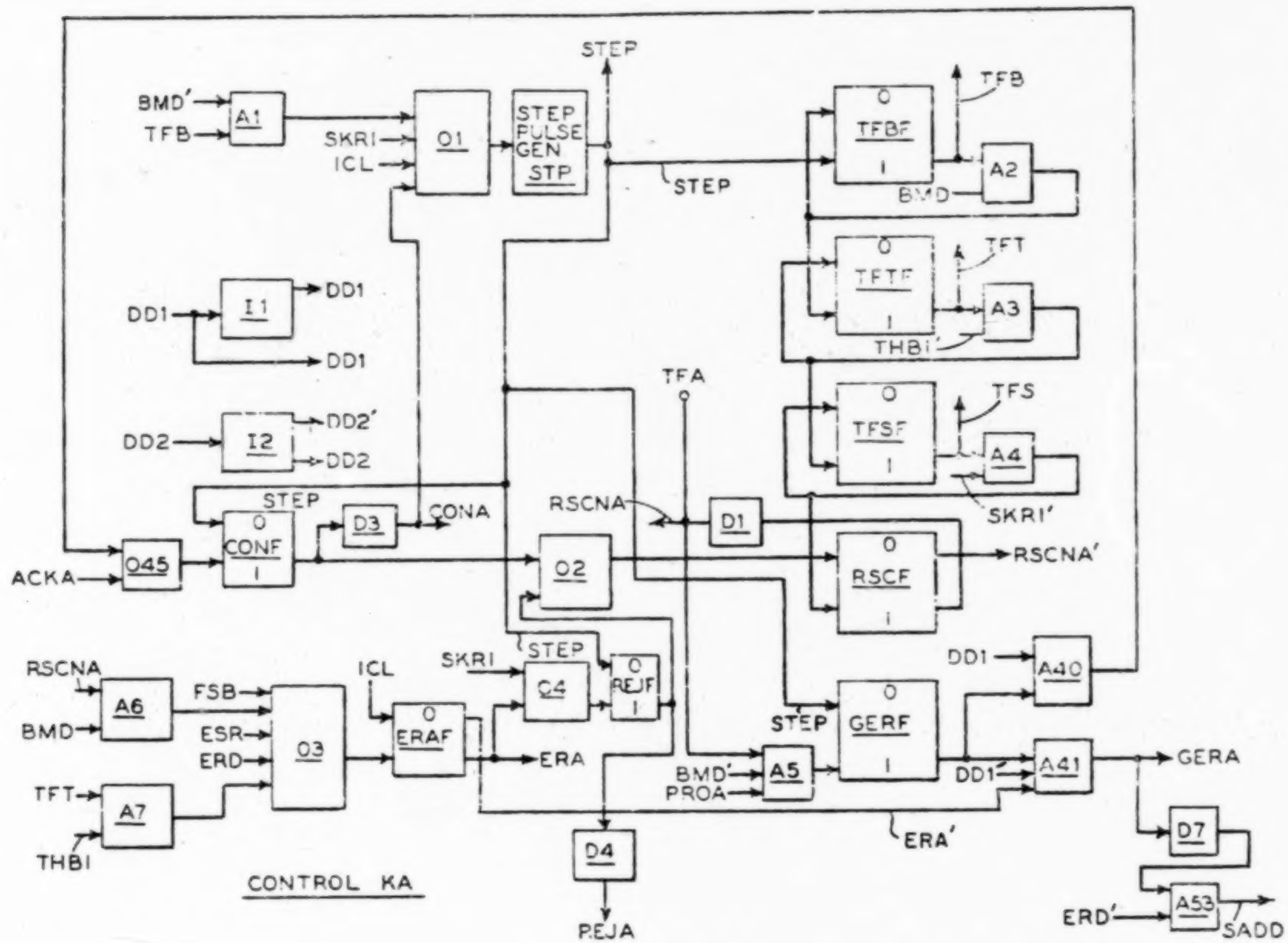
FIG. 2



TRANSACTION PROCESSOR MRA

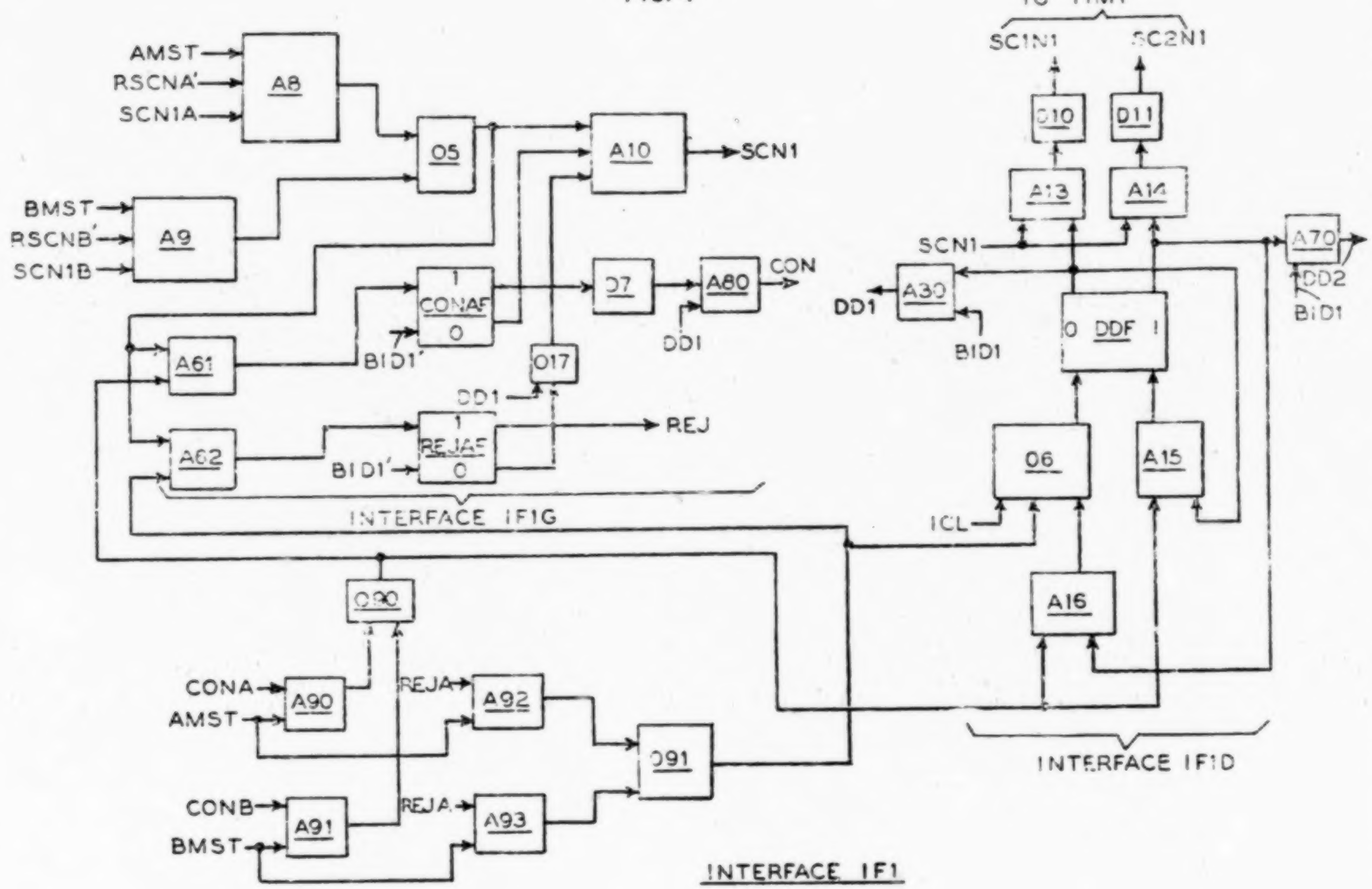
May 17, 1966
R. L. WEIDA ETAL
3,252,149
Filed March 28, 1963
DATA PROCESSING SYSTEM
5 Sheets-Sheet 4

FIG. 3



May 17, 1966
Filed March 28, 1963
R. L. WEIDA ETAL
DATA PROCESSING SYSTEM
3,252,149
5 Sheets-Sheet 5

FIG. 4



3,252,149

DATA PROCESSING SYSTEM

Robert L. Weida, Whitestone, Edward M. Richards, East Northport, Evelyn Berezin, New York, Jack Knoll, Plainview, and Philip Rosenblatt, Mount Vernon, N.Y., assignors to Digitronics Corporation, Albertson, N.Y., a corporation of Delaware

Filed Mar. 28, 1963, Ser. No. 268,743
33 Claims. (Cl. 340—172.5)

This invention pertains to data processing systems and more particularly to systems for processing data received from ticket issuing machines.

One of the most common of these systems is a parimutuel system employed for servicing transactions or wagers made by spectators at sporting events. Presently available systems are slow operating, have only average reliability, depend on considerable human assistance and have limited versatility. It should be particularly noted that such systems can neither tolerate any down time during the course of wagering by the spectators, nor can it tolerate any errors in the processing of the wagers.

It is a general object of one aspect of the invention related to the problem of down time and reliability to provide an improved parimutuel system.

Briefly in accordance with this aspect of the invention a data processor is provided for processing transactions having a plurality of pairs units. Each of the units of the pair concurrently performs the same functions. However, one unit is the master unit and the other the slave unit. A master selecting means initially selects which unit of a pair of units is the master unit and which is the slave unit. The master selecting means can instantaneously change the slave unit of a pair of units to the master unit of that pair of units whenever it receives an erroneous-transaction indicating signal from the master unit of that pair. Checking means are included in each unit of the pairs for checking for erroneous transaction signals so as to transmit an erroneous-transaction indicating signal to the master selecting means.

Features of this aspect of the invention include: various checking means for detecting erroneous transaction signals; means for deactivating the data processor when the checking means in both units of a pair detect erroneous-transaction signals; means for comparing the results obtained by each unit of a pair for equality so as to deactivate the data processor if an inequality exists; means for synchronizing the units of a pair of units to each other; and means for rendering ineffective the unit of a pair of units which detected erroneous-transaction signals.

high speed scanning means for interrogating

It is a general object of another aspect of the invention to provide a more versatile system. Briefly, in view of this a plurality of relatively slow operating ticket issuing machines for transactions.

Briefly, in accordance with this aspect of the invention, scanning means are provided for sequentially and periodically selecting each of the ticket issuing machines for interrogation. Interrogating means transmit an interrogation signal to the selected ticket issuing machine. If the selected ticket issuing machine is prepared to make a transaction it will transmit a selected transaction signal. Means sense for the transmission of the selected transaction signal which if not sensed causes the scanning means to immediately step to another ticket issuing machine for interrogation.

A feature of this aspect of the invention is to insure that succeeding attempted interrogations by the scanning means of a ticket issuing machine which has had its transaction confirmed or rejected do not cause the transmission of redundant selected transaction signals.

It is a general object of another aspect of the invention to provide a more versatile system. Briefly, in view of this

aspect of the invention, apparatus is provided for processing sequential multientry transactions such as, but not limited to, daily doubles. The apparatus includes means for insuring that the first entry is first received and only transferred to a storage means and that the second entry is then received. Address generating means only then accept the first entry stored in the storage means and the second received entry to generate a storage address which is used to select a storage register associated with the particular first and second entries.

Other objects, features and advantages of the invention will be apparent from the following detailed description of the invention when read with the accompanying figures wherein:

FIGS 1A and 1B show a parimutuel system as an exemplary embodiment of the invention;

FIG. 2 shows the transaction processor MRA of the system of FIG. 1;

FIG. 3 shows in logical symbols the control KA of the message register MRA of FIG. 2; and

FIG. 4 shows the interface IF1 of the parimutuel system of FIG. 1.

The system includes a plurality of ticket issuing machines which accept transactions on entries in a contest such as a horse race. At least one of the ticket issuing machines will handle what is commonly known as a daily double transaction. The transactions are operated upon by a data processor. The data processor includes common units such as a console C, first and second inequality testers DU1 and DU2, and output units OU. The data processor further includes pairs of units such as scanners SCA and SCB, buffers 1A to NA, and 1B to NB, transaction processors MRA and MRB, and transaction calculators TCA and TCB. Generally, the system is set up so that one unit of each pair will operate as a master and the other as a slave. This is called the dual mode. However, it is possible to initially set up the system so that just one unit of each pair operates and the other is idle. This is called the simplex mode.

Each transaction calculator TCA and TCB includes a plurality of registers a portion of which are aggregator registers; aggregated transaction updating means, a computer, an error unit and an acknowledge unit.

The system will be described operating in the dual mode with the A side as the master. It should be noted that the left hand units of the pairs in FIGURE 1 have a reference character terminating with the letter A and these units comprise the A side. Similarly, the right hand side is the B side.

A switch in the console C will generate the AMST and AMSTC signals fed respectively to the transaction processor MRA and the transaction calculator TCA, indicating they are the masters. In addition the AMST signal is fed to all of the interfaces IF1 to IFN so that scanner SCA will control the sequential and periodic interrogation of the ticket issuing machines TIM1 to TIMN. In spite of this fact, scanner SCB will follow along to instantaneously take over in case of emergency as is hereafter more fully described. In any event, each transaction processor MRA and MRB will concurrently process a transaction; i.e. check for erroneous transactions and other internally generated errors, and generate storage addresses for the memory positions in the ticket issuing machine memory whose contents are to be updated and also the addresses of the aggregator registers in the transaction calculators TCA and TCB whose contents (the aggregated transactions) are to be updated. While both transaction processors MRA and MRB both process the transactions, only the processed transaction information from the master transaction processor is fed to both transaction calculators TCA and TCB. Both the transaction calculators TCA and TCB operate on the processed

transaction information to calculate odds, pools, payoffs and similar information. However, because transaction calculator TCA is the master by virtue of the AMSTC signal from console C, only its result information is fed to the various output units OU.

Transaction calculator TCB follows along to immediately take over if there is a failure in transaction calculator TCA. Of course it is understood that side B could equally be the master. Furthermore, there can be a split; i.e. scanner SCA and transaction processor MRA, and transaction calculator TCB being the masters whereas scanner SCB and transaction processor MRB, and transaction calculator TCA being the slaves or vice versa. What should be understood, however, is that while one of the units of a pair controls the flow of information, the other unit of a pair operates both as an on-line standby unit to immediately, either partially or entirely, be switched into the circuit if failures occur in the master unit of the pair and also to perform a check on the master unit of the pair.

All units are connected by signal lines which transfer signals between the units. It should be noted that the signal lines bear the same reference characters as the signals on the lines and that this terminology is used interchangeably. Accordingly, when only the signal has been mentioned, the signal line is implied and vice versa. Furthermore, some signals are shown in a single line for the sake of convenience in spite of the fact that they are a plurality of lines in a cable. The lines AADR, WADR, MOA, MIA, SKNA and SKRN are typical examples. In addition the lines shown only indicate one

the

polarity of this signal such as the BID1' signal. However concurrent with this signal line there are instances where there is a parallel signal line carrying the opposite polarity of this such as the BID1' signal.

Switches on the console C determine which side is master, say the A side, by positioning the SMST switch to the A position which generates the AMST and AMSTC signals, initially clear the system (the ICL signal) by momentarily depressing the initial clear switch SIC, and indicate the entries upon which no transactions will be allowed by positioning the appropriate non-transaction switches SKWN which respectively generate the associated non-transaction signals SKRN. These would be "scratches" in a horse race.

The AMST signal fed to the interfaces IF1 . . . IFN (only two of which are shown, although there are many) sensitizes these units to interrogating signals such as the

the SCN1B signal from

SCN1A signal from the scanner SCA and not the scanner SCB although both are simultaneously present at an interface. The AMST signal fed to transaction processors MRA and MRB insures that storage address signals are fed only from the transaction processor MRA to registers MEMA and MEMB and ticket issuing machine memory WM. Similarly the AMSTC signal fed to the transaction calculator TCA insures that only its result information is fed to the output units OU.

The ICL signal fed at least to the transaction processors MRA and MRB preset the scan counters SKA and SKB (a typical one being shown in FIGURE 2) to their initial count of one. The outputs of the scan counters SKA and SKB are fed as the SKNA and SKNB signals respectively from transaction processors MRA and MRB to scanners SCA and SCB. The SKNA and SKNB signals are decoded by the scanners SCA and SCB and become respectively the SCN1A and SCN1B signals which only go to interface IF1. If the ticket issuing machine TIM1, which is the daily double machine, wishes to make a transaction then one of its transaction keys from each bank will be depressed and BID1 signals will be received by the interface IF1 which has no effect at this time. A DD1 signal indicating that this is the first entry of a daily double transaction is fed to the transaction processors MRA and MRB. The scan is now at ticket issuing machine TIM1 for interrogation of the

first entry of the daily double transaction. The SCN1A signal passes to the ticket issuing machine TIM1 as an SC1N1 signal which is fed to the common side of all of the transaction-selection switches of the first bank in ticket issuing machine TIM1 (see FIG. 4). This signal will pass through to the other side of the closed transaction selection switch of the first bank and is fed out as a selected transaction HN1 signal to buffers NA and NB (N is actually the number of the entry or the number of the depressed entry key). For example, if the first entry of the daily double transaction is being inserted on entry 1, the entry key 1 of the first bank would have been depressed, causing the closing and latching of the associated transaction-selection switch and an H11 signal would be fed through buffers 1A and 1B to become respectively the particular entry H1A and H1B signals fed to both the transaction processors MRA and MRB respectively. The H1A signal is stored in the entry register 1HRA and also and more particularly in the entry register 2HRA (FIG. 2) under the control of the DD1 signal. The H1B signal is stored in an identical entry register 2HRB (not shown) of transaction processor MRB.

It should be noted that unless specifically indicated otherwise, whatever applies to the transaction processor MRA also applies to the transaction processor MRB, since both of these units are identical and perform concurrent processing steps.

At the same time, control KA (FIG. 2) transmits a test for transaction made TFB signal generated by flip-flop TFBF (FIG. 3) to probe the transaction made unit BMA. If a transaction has been made as indicated by the presence of a signal on one of the HNA lines, a BMD signal is fed back to control KA to start an error test routine. If no BMD signal is fed back, control KA generates a STEP signal to scan counter SKA which steps to the count of 2 to initiate the transaction interrogation of ticket issuing machine TIM2. The detailed operations associated with the STEP signal will be described hereinafter. It should be noted that the HNA signal was derived from the SC1N1 signal passing through a latched transaction switch and if this switch was not latched the STEP signal was generated. Therefore, this is the method for stepping over ticket issuing machines which are not prepared to perform a transaction.

However, assume, as we have, that one of the transaction selection switches was latched. Therefore one of the HNA signals is present, causing the transmission of a BMD signal to control KA. Therefore, the error test routine starts. In particular, the presence of the BMD signal at an input of and unit A2 passes a pulse to the set to "1" input terminal of flip flop TFTF which generates the TFT signal and to the set to "0" terminal of flip flop TFBF (FIG. 3). The first test of the error test routine after the test for bet made process step is a two entry transaction test, i.e. a test is made to insure that the signals from entry register 1HRA indicate only one entry is stored therein. It could conceivably happen that ticket issuing machine TIM1 faultily transmitted both the H11 and H21 signals at the same time or that through a failure in the buffers 1A and 2A both the H1A and H2A signals are transmitted to the entry register 1HRA. In such a case, the two entry transaction test unit THBA (FIG. 2) will reply with a THBI signal in response to the TFT signal from control unit KA. If such is the case, control KA sets the error flip-flop ERAF generating the ERA signal (FIG. 3) and generates the REJA signal. The detailed operations of the ERA and REJA signals are hereinafter more fully described. For the time being it is only necessary to know that the REJA signal results in the unlatching of the latched transaction selection key in the ticket issuing machine TIM1 and that the ERA signal will render the message register MRA ineffective. The ERA signal is fed to the transaction processor MRB, inequality tester DU1

and the console C to perform functions which are hereinafter more fully described.

If no such error is detected a THBI' signal is fed to one input of and unit A3 whose output is fed to the set to "0" input of flip-flop TFTF and to the set to "1" input of flip-flop TFSF which generates the TFS signal to test for the selection of an entry upon which no transaction will be accepted is now made. This is in racing parlance a scratch test. The signal representing the entry stored in the entry register 1HRA (FIG. 2) is fed as one of the 1HRN signals to the test for non-allowed transaction unit TFSA and are compared with the non-transaction signals SKRN from console C. The TFS signal from control KA probes for equality which if it exists causes the return of a SKRI signal to control KA which generates a REJA signal. It also causes the generation of an STEP signal fed to scan counter SKA for stepping the scan to the ticket issuing machine TIM2. If no non-allowed transaction is detected the next error processing step is performed. In particular, a SKRI' signal is fed to one input of and unit A4 whose output is fed to the set to "0" input of flip-flop TFSF and the set to "1" input of flip-flop RSCF which generates the RSCNA' signal. This starts the false entry test which ensures that the signal on one of the lines HNA truly resulted from the depressing of an entry key. The signal RSCNA' is fed from transaction processor MRA to all the interfaces. However, since the scan is at ticket issuing machine TIM1 (the SCN1A signal), it passes through interface IF1 where it terminates the generation of the SC1N1 signal (see FIG. 4). It will be recalled that the SC1N1 signal was the interrogating signal which passed through the latched transaction selection switch causing transmission of signals through buffers 1A to NA and 1B to NB to indicate which entry a transaction was being made upon. Therefore none of the lines HNA should carry a signal when the SC1N1 signal is absent. After a delay to permit the passage of signals through the loop including the ticket issuing machine TIM1, the RSCNA signal is fed to the transaction made unit BMA (FIG. 2). At this time if no signals are on the lines HNA a BMD signal is not generated. If however the BMD signal, indicating one of the HNA signals must be present, is generated, control KA will receive this signal which causes the setting of the error flip-flop ERAF and the generation of the ERA and REJA signals in the usual manner.

During this test a synchronizing operation is performed. It will be recalled that in the case under discussion, the A side is the master but the B side follows along. Therefore, it is necessary to keep the scanners SCA and SCB in step so that if the A side (master) drops out the B side picks up exactly where the A side left off. Therefore, since there may be some differences in the time to perform the error processing by each of the transaction processors MRA and MRB because there is no overall master synchronization, these processors are synchronized to each other. It should be noted that an overall master synchronization would defeat the independency of the sides. Therefore, when either transaction processor completes a test routine it generates a signal indicating this fact. For example, after tests are made for test for bet made, the test for two-entry transaction, and the test for non-allowed transactions and concurrent with the test for a false entry transaction, the test-finished TFA signal is generated by control KA (FIG. 3) and is fed to the synchronizer SYNA (FIG. 2). The TFA signal is also transmitted to the analogous synchronizer SYNB in the transaction processor MRB. When the transaction processor MRB reaches this same point, it transmits the TFB signal to the synchronizer SYNA. At this time, the coincidence of the TFA and TFB signals cause the generation of a PROA signal which is fed to the control KA to initiate the next processing step. Although for the sake of simplicity this synchronization is shown as taking place at only one processing step, it preferably occurs at each of the processing steps. In this manner the scanners SCA and SCB stay in step. However, if an error occurs in a transaction processor, it will be rendered ineffective. Therefore it will not generate succeeding test or step-finished signals, but since it generates an error signal this signal is used to replace the test-finished signal. For example, assume transaction processor MRB detected an error. It would "shut down" and start generating the ERB signal. The ERB signal is received at synchronizer SYNA and replaces the TFB signal. Therefore, a PROA signal will be generated whenever a TFA signal is generated. After all these error tests have been completed, a GERF flip-flop is set (FIG. 3). In particular, the coincidence of the PROA signal, the BMD' signal (indicating that there has been no false entry) and the RSCNA signal (the delayed "1" output of the RSCF flip-flop) at inputs to and unit A5 set the GERF flip-flop to "1." The "1" output of the GERF flip-flop is passed via and unit A40 because of the presence of the DD1 signal and is fed by the or unit O45 to the set to "1" input of the CONF flip-flop. The "1" output of the CONF flip-flop passes through or unit O2 to the set to "0" input of the RSCF flip-flop which again generates the RSCNA' signal which is fed to the interface IF1 to regenerate the SCN1 signal (see FIG. 4). Although the SCN1 signal passes through and unit A13 to again cause the generation of the SC1N1 signal which causes an entry to be accepted by entry register 1HRA as described before, it should be noted that this is the same entry as before, so it makes no difference. The "1" output of the CONF flip-flop passes through delay unit D3 to become the CONA signal which is also fed to interface IF1. The CONA signal passes through and unit A90 to an input of or unit O90. The output of or unit O90 is fed via and unit A15 (FIG. 4) to the set to "1" input of the daily double flip-flop DDF. The "1" output is gated by the BID1 signal at and unit A70 causing the generation of the DD2 signal and the "1" output gates the SCN1 signal through the and unit A14 to the delay unit D11. Delay unit D11 delays the generation of the SC2N1 signal which is used to probe the second bank of transaction selection switches. However, because of the delay, the sampling has no effect because the DD1 signal is no longer present when the SC2N1 signal is generated. The absence of the DD1 signal at and units A20 and A21 in FIG. 2 prevents the passage of the second entry into the entry register 2HRA.

The CONA signal is also fed via and unit A90, or unit O90 and and unit A61 to the set to "1" input of the CONAF flip-flop. Since the "1" output of the CONAF flip-flop is delayed by delay unit D7, the DD1 signal disappears before this "1" output reaches and unit A80, therefore no CON signal is generated at this time.

The CONA signal passes through or unit O1 (FIG. 3) to trigger the step pulse generator STP which is a conventional delay multivibrator to generate the STEP signal which accordingly occurs after the CONA signal. Therefore the scan counter SKA steps to a count of 2 so that the ticket issuing machine TIM2 may be interrogated. When the scan steps off ticket issuing machine TIM1 the BID1 signal terminates, causing the generation of the BID1' signal which is connected to the set to "0" inputs of the CONAF and REJF flip-flops (FIG. 4). REJAF

The step signal STEP clears the entry register 1HRA (FIG. 2) as well as setting the TFBF flip-flop to its "1" state, and the CONF flip-flop, the REJF flip-flop and the GERF flip-flop to their "0" states.

It should be noted that at this point only the first entry of the daily double transaction has been processed. When the scan again returns to the ticket issuing machine TIM1 the second entry of the daily double transaction is processed. When the SCN1 signal is generated as previously described, it passes through and unit A14 to cause the generation of the SC2N1 signal (FIG. 4) which probes the second bank of entry keys causing the second entry to enter the entry register 1HRA in the usual manner. It

A268

should be noted that this entry does not pass to the entry register 2HRA (FIG. 2) because of the absence of the DD1 signals at the and units A20 and A21. The same series of processing steps are performed by the process step flip-flops as before until the GERF flip-flop is set to its "1" state. This time the presence of the DD1' signal at and unit A41 causes the "1" output of this flip-flop to become the GERA signal. Note that the "1" output does not pass through the and unit A40 because the DD1 signal is absent.

The GERA signal strobes the storage address generator SAGA (FIG. 2). The storage address generator SAGA is a plurality of and units each having one of its inputs connected to the GERA signal line and other inputs connected to various combinations of the 1HR1 . . . 1HRN, 2HR10 . . . 2HRN0, and DKN signal lines from decoder DEC.

The storage address register SAGA in response to the GERA signal transmits two groups of signals. The first group AADRA1 . . . AADRAM is associated with entry transactions; the second group AADRAM+1 to AADRAN are associated with the ticket issuing machines. These signals are grouped into a cable generalized as an AADRA signal. The AADRA signals are fed to the inequality tester DU1.

It will be recalled that the transaction processor MRB is simultaneously performing the same processing. The AADRA and AADRB signals are checked for inequality by inequality tester DU1 (FIG. 1). If they do not agree then inequality tester DU1 transmits an ERD signal to both transaction processors MRA and MRB. When the controls KA and KB thereof respectively receive this signal they cause the ineffectuation of the transaction processors MRA and MRB respectively and cause the generation of the ERA and ERB signals respectively which are fed to console C, their coincidence being an ambiguity signal which causes the deactivation of the system and gives an alarm.

If, however, these generated storage addresses represented by the AADRA and AADRB signals agree, the ERD signal is not generated and control KA generates the send address signals SADD. In particular the ERD' signal gates the GERA signal delayed by delay unit D7 through and unit A53 (FIG. 3). In FIG. 2 the SADD signal is received by the aggregator address transmitter AATA and ticket issuing machine transmitter WATA. If transaction processor MRA is the master transaction processor as indicated by the AMST signal present at an input to aggregator address transmitter AATA the first and second groups of the storage address signals AADRA pass therethrough to become the aggregator AADR signals. Likewise, the second group of AADRA signals pass through the ticket issuing machine transmitter WATA to becomes the memory position address WADR signals. Similarly, if the B side is the master (the presence of the BMST signals) then the second group of the AADRB signals becomes the WADR signal, and the first and second groups of the AADRB signals become the AADR signals.

From this point onward the operation is no different for a single entry transaction or for a daily double transaction. Therefore, the single entry transaction processing will be described up to this point.

The non-daily double transaction processing, i.e., single entry transaction, is effectively the same as the second entry of a daily double transaction and only the differences will be described. There are no DD1 and DD2 signals generated in the interface IFN of a non-daily double ticket issuing machine TIMN. Therefore, the single entry transaction only enters the entry register 1HRA. Note the DD1 signal is not present at and units A20 and A21 (FIG. 2).

Since the DD2' signal is present and the DD2 signal is not present at inputs of storage address generator SAGA only the 1HR1 to 1HRN signals, and the DKN signals will be included in the AADRA signals.

In the dual mode with both transaction calculators TCA and TCB operating the AADR signal is fed to both registers MEMA and MEMB. The addressing circuitry therein receives the aggregator address signals AADR to select the indicated aggregator register. The contents of the selected aggregator address are read out, recirculated and written back into the same selected aggregator register to update the number of transactions. In particular, for example, the AADR signals when received by the aggregator registers of registers MEMA selects the column associated with the ticket issuing machine and the row associated with the particular entry upon which a transaction is being made. The signals representing the accumulated number of transactions in that aggregator register are read out via MOA signal lines to the updater UAA where the count they represent is updated by 1 and then fed back via the MIA lines to the original aggregator register in registers MEMA. At this time, registers MEMA feed an acknowledgment ACKA signal via amplifier AKA, indicating the transaction has been recorded, to the control KA.

The ACKA signal, whether as a result of a daily double transaction or a single entry transaction, passes through, or unit O45 (FIG. 3) to set the CONF flip-flop to the "1" state and the resulting procedure described for such a condition during the entry of the first entry of the daily double transaction procedure occurs with minor differences. Since the DD1 signal is not present at and unit A80 (FIG. 4) the "1" output of the CONAF passes therethrough to become the CON signal which is fed to the ticket issuing machine under scan causing the unlatching of the switches and the issuing of the ticket receipt. If the daily double ticket issuing machine TIM1 is under scan then the CONA signal also passes via and unit A14 A16 and or unit O6 to the set to "0" input terminal of daily double flip-flop DDF so that it is prepared to receive the first entry of a new daily double transaction at a later time. It should be noted that non-daily double interfaces only include the interface IF1G portion of FIG. 4. Furthermore, the CON signal is taken directly from the "1" output of the CONFA flip-flop. Therefore and unit A80 and delay unit D7 may be deleted. CONAF

Of course, all this time, transaction calculator TCB and registers MEMB are performing the same operations resulting in the generation of an ACKB signal fed to transaction processor MRB. However, it should be noted that since the A side is the master the AMAST signal is present at interface IF1 and therefore the CONA signal from transaction processor MRA does the confirming, in spite of the fact that the CONB signal from transaction processor MRB is also fed to the interfaces.

While the entry transaction is being aggregated the specific ticket issuing machine transaction is also aggregated. In particular, the WADR signal is fed to ticket issuing machine memory WM. The specific addressed memory position therein is selected in a manner described above for the registers MEMA and the contents of that addressed memory position are read out on the WO signal lines and fed via the updater UAW and the WI signal lines back to the same addressed memory position in the ticket issuing machine memory WM. In this way, a central check is maintained on the number of transactions made by each ticket issuer. For the sake of simplicity there has been shown only an aggregation of the total transactions made by a ticket issuer. The routine can obviously be refined to also indicate the specific activity on each entry.

The transaction processors MRA and MRB continue in this maner to sequentially interrogate each ticket issuing machine TIMN and process any transactions that are made. Finally, the scan counters SKA and SKB reach a count that is one greater than the number of ticket issuing machines TIMN. Therefore, no ticket issuing machine is interrogated on this step. Instead, the reliability of the buffers NA and NB are tested for short circuit conditions which would effectively prevent transactions on certain

A269

entries during certain periods of time. For example, if an element in buffer **1A** associated with the line **H11** is short circuited and the entry number **1** key of ticket issuing machine TIM1 is depressed while the scanner SCA is pointing to any other ticket issuing machine such as TIMN then this other ticket issuing machine will not be able to have a transaction processed on entry **1**.

The test is performed by transmitting the CHKA signal derived from the SCNZA signal generated by scanner SCA to each of the buffers NA. For simplicity,

$$CHKA=SCNZA$$

Buffers NA should each transmit a simulated transaction on each entry, i.e. signals should be present in all lines H1A . . . HNA. The lines H1A . . . HNA are all fed to the end scan test ESTA (FIG. 2) and a multicoincidence is tested for by the SCNZA signal. If the multicoincidence is not obtained an ESR signal is fed to control KA causing the generation of the ERA error signal (FIG. 3).

During all the time up to the start of the race the computers COMA and COMB periodically perform calculations on the aggregated transactions to establish interim accounting results such as odds. In particular, each computer has access to the aggregator registers which supply the operands. Error checking, such parity checks, for example, are performed during these calculations. If an error is detected by either transaction calculator it generates an error signal. For example, if transaction calculator TCA detects an error it will become ineffective and cause error unit ERCA to generate a CERA signal. Similarly, for transaction calculator TCB. If transaction calculator TCA is the master as indicated by presence of the AMSTC signal from console C and transaction calculator TCB detects an error, it becomes ineffective but there is no change of master and slave. It should be noted though that the CERB signal is generated. If, however, transaction calculator TCA detects the error, the CERA signal when received by console C terminates the AMSTC signal and generates the BMSTC signal making computer B the master. The CERA and CERB signals are also fed to inequality tester DU2. The presence of either of these signals disables inequality tester DU2.

In any event, if there is no calculator error when an output is desired each transaction calculator TCA and TCB transmits the result information via the lines POUA and POUB to the inequality tester DU2 where an inequality check is performed. If an inequality in the result information is found, inequality tester DU2 generates the CERD signal which is fed to both errors units ERCA and ERCB which generate the CERA and CERB signals respectively. The coincidence of the CERA and CERB signals is an ambiguity signal to console C which deactivates the system. If equality is found, then the master transaction calculator, in the case under discussion, transaction calculator TCA, transmits the output information to the output units OU.

The effect of the setting to "1" of the error flip-flop ERAF will now be discussed. The error flip-flop ERAF will be set to "1" if: there is a false entry error indicated by coincidence of the RSCNA and BMD signals at inputs of and unit A6; there is a two entry error indicated by the coincidence of the TFT and THBI signals at inputs of and unit A7; a short circuit in one of the buffers [B]NA as indicated by the ESR signal from end scan test unit ESTA; an inequality error indication (the ERD signal) from inequality tester DU1; or when an FSB signal is received from console C indicating simplex mode with only the B side operative. The outputs of and units A6 and A7 and the FSB, ESR and ERD signals feed inputs of or unit O3 whose output is connected to the set to "1" input of error flip-flop ERAF. The setting of the error flip-flop ERAF at any time causes the transaction processor MRA to be ineffective, i.e. "drop out." The ERA signal is sent to console C, which, if an ERB signal is not received from transaction processor MRB, will terminate the generation of the AMST signal only if the A side is the master and

start the generation of the BMST signal. (If the B side is the master, as indicated by the generation of the BMST signal, the BMST is still generated.) In such a case, i.e. the A side is master, at least a portion of the B side, that is, the scanner SCB and the transaction processor MRB will become the master and carry on, and the scanner SCA and transaction processor MRA will perform no effective function in the operation. If any time thereafter the ERB signal is received by console C the system is deactivated. In other words, even if the inequality tester DU1 does not detect an inequality it is possible for the system to shut down. This can occur when the master detected an error and the slave took over, and then the slave detected an error; or when the slave first detected an error and then the master detected an error. This is known as a joint error. The ERA signal is fed also to the transaction processor MRB and to the inequality tester DU1. Generally, the ERA signal fed to the inequality tester DU1 disables it since there will be no further need to perform such a test between the outputs of the transaction processors MRA and MRB. In fact, if this were not done, then the inequality tester DU1 would generate an ERD signal causing the deactivation of the system. Similarly, the ERA signal fed to transaction processor MRB "disables" a synchronizing circuit SYNB therein since synchronization is no longer required between the transaction processors MRA and MRB as heretofore described. The "0" output of the ERAF flip-flop ERA' is fed to an input of and unit **A41** to prevent the generation of a GERA signal so that no storage address will be generated by the storage address generator SAGA. The ERA' signal will also pass through or unit O4 to the set to "1" input of the REJF flip-flop to initiate a reject routine.

The effect of the REJA signal will now be described. The REJF flip-flop will be set to "1" whenever the non-allowed transaction signal SKRI or the error signal ERA is generated (see FIG. 3). The ERA signal and the SKRI signal are fed via or unit O4 to the set to "1" input of REJF flip-flop. The "1" output thereof is fed via or unit O2 to the set to "0" input of the RSCF flip-flop causing the generation of the RSCNA' signal which is fed to interface IF1 (FIG. 4), for example. This signal will pass via and unit A8 and or unit O5 to one input of and unit A62. The "1" output of REJF flip-flop passes through delay unit D4 to become the REJA signal (FIG. 3) which is also fed to interface IF1. Signal REJA passes via and unit A92 and or unit O91 to the second input of and unit A62 whose output is connected to the set to "1" input of the REJAF flip-flop causing the generation of the REJ signal which is fed to ticket issuing machine TIM1 to unlatch the latched switch. The output of or unit O91 is also fed via or unit O6 to the set to "0" input terminal of daily double DDF flip-flop to prepare it to generate the DD1 signal when a daily double transaction is to be made.

There will now be discussed the generation of the STEP signal when: there is no error; and when no CONA signal has been generated as a result of the valid processing of the first entry of a daily double transaction or the valid processing of any transaction resulting in the issuance of a ticket receipt. If no transaction is sensed or if a non-allowed transaction is sensed it is necessary to step to the next ticket issuing machine without any further processing. The first case is indicated by the presence of the BMD' and TFB signals at inputs of and unit A1 whose output feeds or unit O1. The second case is indicated by the presence of the SKRI signal at a second input of or unit O1. The output of or unit O1 when it transmits a signal in response to a signal received by one of its inputs will cause step pulse generator STP to generate a STEP signal in the usual manner. The role of the STEP signal has been described above.

It should be noted that the scanning is electronically performed and proceeds at high speed whereas the ticket issuing machines are electromechanical and therefore relatively low speed devices. To insure utilization of the

high speed scanning rates the scanners SCA and SCB do not wait until the unlatching of transaction selection switches and the ticket printing is performed before stepping, but, instead, step immediately after initiating these operations. Accordingly, it is possible for the scanners to return to such a ticket issuing machine before the unlatching is complete. Therefore, if no provisions are taken a new transaction will start. Provisions for the prevention of such an error will be described for ticket issuing machine TIM1, which is typical.

Accordingly, it should be noted that as long as a transaction selection switch is latched the BID1 and BID1' signals are generated. It should also be recalled that when the scan stepped at least one of the CONAF or REJAF flip-flops was in the "1" state (see FIG. 4). Therefore, when the SCN1A signal is generated it will pass through or unit O5 to one input of and unit A10 whose other two inputs are connected respectively to the "0" outputs of the CONAF and REJAF flip-flops. If either is set to "1" then and unit A10 will not pass an SCN1, and accordingly no interrogating signal is generated. Therefore, no signals will be on any lines HIA to HNA and the transaction made unit BMA when tested as previously described will not send back a BMD signal to control KA which will immediately generate a STEP signal moving the scan to ticket issuing machine TIM2. In this manner, the rapidly moving scanners can move past the slow operating ticket issuing machines without registering erroneous duplications of the transactions. However, when the transaction switch is finally unlatched the BID1' signal sets the CONAF and REJAF flip-flops (whichever was set to "1" because of a reject or confirm) to the "0" state. The next time the scan reaches ticket issuing machine TIM1 an interrogation will be performed. However, during a daily double transaction, after the first entry is processed the transaction switches will remain latched and remain so until after the second entry is processed. Therefore, the DD1 signal is fed to one input of or unit O17 to override the effect of the "0" output of the CONAF flip-flop.

DESCRIPTION OF THE ELEMENTS OF THE SYSTEMS

Daily double ticket issuing machine TIM1 may be of the type which includes two banks of entry keys each associated with a different entry. Each of these keys when depressed closes a transaction selection switch which latches. Each of the switches is effectively of the single-pole single-throw type having a moving contact electrically connected to a common input line, and a fixed contact connected to a selected output line such as line H11. The common input line for the first bank is the SC1N1 signal line and the common input line of the second bank is the SC2N1 signal line. The outputs of similar transaction selection switches of each bank are connected together to the same output lines. It should be noted that non-daily double ticket issuing machines have only one bank of entry keys and associated transaction selection switches. Such machines receive only the SCN1 signals. Ganged to all these switches is a bid switch which generates BID1 and BID1' signals as long as any transaction selection switch is latched. Included in the ticket issuing machine is an electromechanical ticket issuing and printing mechanism which is energized by the confirming CON signal to print and issue a ticket and unlatch any transaction selection switches. There is also electromechanical means for unlatching the switches upon receipt of a reject REJ signal.

A typical buffer **1A** for entry **1** includes the logical elements which satisfy the Boolean equation:

$$(H11+H12\ .\ .\ .\ H1N+CHKA)=H1A$$

where N is associated with the ticket issuing machine TIMN.

A typical scan counter SKA is a chain of conventional cascaded binary counters wherein each binary counter

has an output from both its "1" and "0" sides such as those shown in the section entitled Binary Counting, starting on page 194 of "Arithmetic Operations in Digital Computers" by R. K. Richards, published by Van Nostrand, New York in 1955. The output of the first counter would be SK1A and SK1A', etc. These lines are generalized in a single cable referred to as SKNA.

The typical scanner SCA is a decoder which decodes the combinations of "1's" and "0's" from the scan counter SKA. It may be of the type shown in the section entitled Matrices starting at page 71 of the book "Arithmetic Operations in Digital Computers" wherein FIG. 3–3(*a*) is suitable when extended to the appropriate number of binary counters in scan counter SKA. It should be noted that each letter A, B or C in FIGURE 3–3(*a*) is associated with a different binary counter stage, i.e., A is associated with the first binary counter stage, B the second, etc. and where an unbarred letter (A) is the "1" output of the binary counter and the barrel letter ($\bar{A}$) is the "0" output barred of the binary counter. In the terminology used herein $\bar{A}=A'$.

The console C includes at least a plurality of transaction prevention switches SKW each associated with a different entry upon which no transactions will be accepted. For example, if entry 1 is to be excluded then the appropriate switch SKW1 is closed to transmit a non-transaction signal on the line SKR1 of the SKRN signal line cable. The console C further includes an initial clear switch which generates an ICL signal for clearing various control elements as well as clearing the scan counters SKA and SKB to a start count. The master determining means may be two flip-flops such as the type shown in FIG. 2–15(*a*) on page 48 of said "Arithmetic Operations in Digital Computers" book, may be employed to generate the AMST and BMST signals, and the AMSTC and BMSTC signals. In one case the "1" output generates the AMST signal and the "0" output the BMST signal. The left hand input (the set to "0" input) receives the ERA signal and the right hand input (the set to "1" input) the ERB signal. These inputs will normally initially receive a signal from a switch for setting up the A master or B master modes. The other case for generating the AMSTC and BMSTC signals is analogous. A logical element such as an and unit will sense for the coincidence of the ERA and ERB signals (the coincidence of these signals can be considered the ambiguity signal) for deactivating the system and giving an alarm. Similarly an and unit is included to test for the coincidence of the CERA and CERB signals (an ambiguity signal) to deactivate the system and give an alarm. The console also includes a three position mode switch SFS which: when in the D position indicates the dual mode; when in the A position causes the generation of the FSA signal indicating simplex mode with A the master; and when in the B position generates the FSB signal indicating simplex mode with B the master.

Inequality tester DU1 is essentially a conventional equality comparator which is disabled by the presence of either the ERA or ERB signals. There are innumerable appropriate types available in the existing art.

For example, a logical element satisfying the following Boolean equation can be employed:

$$[ERA'\cdot ERB']\cdot[(\Sigma AADRAN\cdot AADRBN')+(\Sigma AADRAN'\cdot AADRBN)]=ERD$$

where the summation is for all values of N which are the separate output lines of aggregator address generators. The ERD signal is also fed to an inverter to generate the ERD' signal.

Inequality tester DU2 is a logical element which satisfies the following Boolean equation:

$$[(CERA'\cdot CERB')]\cdot[(POUA'\cdot POUB)+(POUA\cdot POUB')]=CERD$$

The CERD signal is also fed to an inverter to generate the CERD' signal.

The registers MEMA and MEMB are identical and include a multiplane magnetic core matrix which is divided into rows and columns wherein the core in each plane in the same row and column provides a bit storage for a multibit binary number. A group of the registers (aggregator registers) is reserved for aggregating transactions. Other registers are reserved for storing opeation and result information of the computer COMA. Included with the registers are typical row and column selectors as well as read and write amplifiers.

Consider now the aggregator registers. Each row of matrix associated with the aggregator registers may be assigned to a different entry and each column to a different ticket issuing machine. Therefore, the AADR signal lines are actually a plurality of lines divided into two groups. The first group are lines associated with the outputs of the particular entry being made and are coupled respectively to the rows. The second group are a plurality of lines associated with the ticket issuing machine being processed. Of course, this can be refined so that each row is associated not with a particular ticket issuing machine but instead with the same category of transaction. For example, in a horse race pari-mutuel system, one row can be associated with all $2 win bets, another row with all $10 place bets, etc. This is a simple matter since each ticket issuing machine generally handles only one such type of bet. Under control of a read signal the bits of the number will be read out of the selected aggregator register as signals on the sense windings connected to the MOA signal lines; passed through a means for updating and returned to the same selected aggregator register under control of a write signal. Such recirculation type magnetic core matrices are well known. For example, typical magnetic core storages may be found in chapter 8 of the book "Digital Computer components and Circuits" by R. K. Richards, published by Van Nostrand, New York, in 1957; or the memory shown in the copending application, Serial No. 223,-481, filed Sept. 13, 1962, for an "Information Transfer System" and assigned to the same assignee.

The means for generating the acknowledge signal can be a logical element satisfying the following Boolean equation:

$$MIA1+MIA2+\ldots+MIAN=ACKA$$

Of course more detailed circuits which include error checking could be employed.

The ticket issuing machine memory WN is a similar multiplane magnetic core matrix and associated units except its matrix may be considered as having a single row. Of course it can have many rows, each associated with different entries.

All the updating means are unit adders which are similar and many are available in the present art. For example, the binary adder shown in FIG. 4–1 of said book "Arithmetic Operations in Digital Computers" can be slightly modified to serve the purpose. In said figure, lines X_3, X_2, X_1 are equivalent to the outputs of the sense windings of the magnetic core planes as represented by the MOA signal lines and the signals S_3, S_2, S_1 are equivalent to the MIA signals lines. The Y_1 signal line is always maintained at binary "1" while the Y_2 and Y_3 signal lines are always maintained at binary "0."

The computers COMA and COMB are identical and may be considered as internally programmed general purpose computers which can perform the necessary arithmetic operations such as odds computations on the aggregated transactions to produce result information such as pay offs. It should be noted that the computers also generate addresses to select the aggregator registers in addition to its own registers. The computers may include conventional parity checking circuits for generating parity error indicating signals as typical error signals. The typical error unit CERA may be a flip-flop as described above wherein the "1" output generates the CERA signal and the "0" output the CERA' signal. The left hand input

ERCA

would be connected to the ICL line and the right hand input connected to the output of an or unit whose inputs are respectively connected to the CERD signal line and FSB signal line.

The output units can take many forms such as visual display boards, line printers, magnetic tape units, etc.

Since the transaction processors MRA and MRB are identical only transaction processor MRA will be described. The entry register 1HRA can be a plurality of flip-flops like those previously described. The left hand input of each of these flip-flops is connected to the STEP signal line. The right hand input of each of the flip-flops is connected to one of the particular transaction signal lines HNA. The "1" output of each flip-flop is connected to one of the 1HRN signal lines. The "0" output of each flip-flop is connected to one of the 1HRN' signal lines. The entry register 2HRA is similar to the entry register 1HRA, except: the left hand inputs of the flip-flops are connected to the output of and unit A40 (FIG. 2); the right hand inputs are connected via the typical and units A20 and A21 to the 1HR1 . . . 1HRN signal lines. The "1" outputs of the flip-flops are connected respectively to the 2HR1 . . . 2HRN lines.

The end scan test unit ESTA may be a logical element satisfying the following Boolean equation:

$$H1A\cdot H2A\cdot\ldots\cdot HNA\cdot SCNZA=ESR$$

The transaction made unit BMA may be a logical element satisfying the following Boolean equation:

$$(H1A+H2A+\ldots HNA)\cdot(TFB+RSCNA)=BMD$$

The BMD signal is fed to an inverter to generate the BMD' signal.

The test for non-transaction unit TFSA is a conventional equality comparator which when strobed by the TFS signal will transmit a SKRI signal if an equality exists. Such a comparator could be a logical element satisfying the Boolean equation:

$$(\Sigma 1HRN\cdot SKRN)\cdot TFS=SKRI$$

where the summation is over all values of N. The SKRI signal is fed to an inverter to generate the SKRI' signal.

The two entry transaction unit THBA can be a conventional majority logical element which will transmit a THBI signal when interrogated by a TFT signal if at least two of the 1HRN signals are coincidently present.

If a majority logical element is inconvenient then a logical element which satisfies the following Boolean equation may be employed:

$$TFT\cdot\{[1HR1\cdot(1HR2+\ldots+1HRN)] +[1HR3+\ldots+1HRN)]+[1HR3\cdot(1HR4 +\ldots+1HRN)]+\ldots +[1HR\ (N-1)\ \cdot 1HRN]\}=THBI$$

The THBI signal is fed to an inverter to generate the THBI' signal.

The storage address generator SAGA will be described for only the case of two possible entries solely for simplicity. In such a case, consider races with only entry 1 and entry 2.

The Boolean equations are for group 1:

$$\begin{aligned} GERA\cdot 1HR1\cdot DD2' &= AADRA1\\ \ldots &= \ldots\\ \ldots &= \ldots\\ GERA\cdot 1HR2\cdot 2HR10\cdot DD2 &= AADRA6 \end{aligned}$$

for group 2

$$\begin{aligned} GERA\cdot DK1 &= AADRA7\\ \ldots &= \ldots\\ \ldots &= \ldots\\ GERA\cdot DKN &= AADRA(N\text{-}6) \end{aligned}$$

where in DKN, N implies the different outputs of decoder DEC.

The decoder DEC is similar to scanner SCA.

The aggregator address transmitter AATA is a logical element satisfying the Boolean equations:

$$\begin{aligned} &(1)\ (AADRA1\cdot SADD\cdot AMST)+(AADRB1\cdot SADD\cdot BMST) &&= AADR1\\ &\quad\ldots &&= \ldots\\ &\quad\ldots &&= \ldots\\ &(M)(AADRAM\cdot SADD\cdot AMST)+(AADRBM\cdot SADD\cdot BMST) &&= AADRM\\ &(M+1)(AADRAM+1\cdot SADD\cdot AMST)+(AADRBM+1\cdot SADD\cdot BMST) &&= AADRM1\\ &\quad\ldots &&= \ldots\\ &\quad\ldots &&= \ldots\\ &(N)(AADRAN\cdot SADD\cdot AMST)+(AADRBM\cdot SADD\cdot BMST) &&= AADRN \end{aligned}$$

The equations (1) to (M) are associated with group 1 and the equations (M+1) to (N) are associated with group 2.

The ticket issuing machine address transmitter WATA is a logical element satisfying the following Boolean equations.

$$\begin{aligned} &(1)\\ &(AADRAM+1\cdot SADD\cdot AMST)+(AADRBM+1\cdot SADD\cdot BMST) &&= WADR1\\ &\quad\ldots &&= \ldots\\ &\quad\ldots &&= \ldots\\ &(N\text{-}M)(AADRAN\cdot SADD\cdot AMST)+(AADRBN\cdot SADD\cdot BMST) &&= WADR(N\text{-}M) \end{aligned}$$

One further comment should be made about the logical elements in the Boolean equations. The symbol "+" implies an or function, the symbol "·" implies an and function and a primed signal implies logical inversion. Many logical elements are available to perform these functions. Typical circuitry for these elements may be found in FIG. 2–2 of said "Arithmetic Operations of Digital Computers" book. In fact, chaper 2 of said book teaches the conversion of Boolean equations to logical elements and the conversion of the logical elements to circuit elements.

The "or" circuit therein can be used for the or units mentioned throughout the specification. The "and" circuit therein can be used for the and units mentioned throughout the specification. In either case non-inverting conventional amplifiers may be connected to the outputs of these units when power amplification is required. When both signals and their inverses are simultaneously required then it may be desirable to employ conventional paraphase amplifiers. The inverters can be conventional signal inverters for inverting direct-current signals. The delay units can be conventional delay elements such as lumped constant delay lines or even delay multivibrators.

Further since the various elements shown in the system are made up of standard components, and standard assemblies, reference may be had to "High Speed Computing Devices," by the staff of Engineering Research Associates, Inc., McGraw-Hill Book Company, Inc., 1950; and appropriate chapters in "Computer Handbook," McGraw-Hill, 1962; edited by Harvey D. Huskey and Granino A. Korn, and for detailed circuitry, to for example "Principles of Transistor Circuits," edited by Richard F. Shea, published by John Wiley and Sons, Inc., New York, and Chapman and Hall, Limited, London, 1953 and 1957. In addition, other references are: for system organization and components: "Logic Design of Digital Computers," by M. Phister, Jr. (John Wiley and Sons, New York); "Arithmetic Operations in Digital Computers," by R. K. Richards (D. Van Nostrand Company, Inc., New York). For circuits and details; "Digital Computer Components and Circuits," by R. K. Richards (D. Van Nostrand Company, Inc., New York).

SUMMARY

The basic system may be summarized as follows: In a system which comprises a plurality of single entry and sequential double entry ticket issuing machines wherein each of said ticket issuing machines comprises:

A plurality of selectively actuatable and latching transaction-selection switches, each associated with a different entry in a race, for transmitting a selected transaction signal associated with the selected entry to an associated output line when the ticket issuing machine receives an interrogating sig al,

A rejection signal responsive means for unlatching any latched switches,

An acknowledgement signal responsive means for issuing a ticket having indicia recorded thereon which is related to a latched switch, and

Means for generating a bid signal when any one of said transaction-switches is latched,

A data processor having a common units and a plurality of pairs of units, each unit of each pair performing the same function as the other unit but with one operating as a master and the other as a slave, said data processor comprising:

(1) a common console means which comprises
 (a) a plurality of selectively actuatable transaction-prevention switches for generating non-allowed signals associated with entries upon which transactions will not be allowed,
 (b) a master selecting means for selecting which unit of each pair of units is a master and which is a slave and for changing the selection upon receipt of an erroneous-transaction indicating signal from the selected master unit, and
 (c) deactivating means for deactivating the system upon receipt of an ambiguity signal or a joint error signal;

(2) one pair of units consisting of first and second scanning means under the control of step signals each comprising
 (a) interrogating means for simultaneously interrogating sequentially and periodically each of said ticket issuing machines to determine if it is to perform a transaction as indicated by a latched transaction-selection switch, and
 (b) transmitting means for transmitting to the latched switch of a ticket issuing machine with a latched switch an interrogating signal from only the scanning means selected by said master selecting means to be the master scanning means;

(3) first and second pluralities of buffer means, each of said buffer means of each of said pluralities having
 (a) one input line connected to one of the associated output lines of each of said ticket issuing machines, and
 (b) one output line for transmitting a particular transaction signal indicating that a transaction is desired on a particular one of the entries;

(4) a second pair of units consisting of first and second transaction processing means each connected respectively to the output lines of said first and secor plu-ralities of buffer means for concurrently processing said particular transaction signals, each of said transaction processing means comprising
 (a) checking means for checking for erroneous transaction signals and for transmitting an erroneous-transaction indicating signal to said console means so that if the master transaction processing means transmitted said signal, said master selecting means selects the slave transaction processing means to be the master transaction processing means, said checking means comprising
  (i) means for testing for the simultaneous presence of more than one particular transaction signal, and

(ii) means for testing for the presence of any particular transaction signals during the absence of said interrogating signals,

(b) comparing means for comparing the particular transaction signals with the non-allowed signals to generate a non-transaction signal and a step signal when a particular transaction signal and a non-allowed signal represent the same entry,

(c) rejection means responsive to an erroneous-transaction indicating signal from said checking means or a non-transaction signal from said comparing means for transmitting a rejection signal to the scanned ticket issuing machine with the latched switch,

(d) no transaction made testing means for testing for the absence of the particular transaction signals during the presence of said interrogation signal for generating a step signal if no particular transaction signals are present,

(e) means responsive to a step signal for advancing the associated scanning means,

(f) synchronizing means for synchronizing processing steps between said first and second transaction processing means comprising

(i) means for transmitting a process step-finished signal to the other transaction processing means when a processing step is finished,

(ii) means responsive to the simultaneous presence of process step-finished signals from both transaction processing means for enabling said transaction processing means to proceed to the next processing step, and

(iii) means responsive to an erroneous-transaction indicating signal from said checking means for disabling said synchronizing means,

(g) generating means for generating storage address signals representing the entry associated with the particular transaction signal and representing the particular ticket issuing machine under interrogation only for non-erroneous particular transaction signals,

(h) transferring means responsive to said master selecting means for transferring said storage address signals as aggregator address signals only from the master transaction processing means,

(i) acknowledgment signal transmitting means for transmitting an acknowledgment signal to the interrogated ticket issuing machine with the latched switch for issuing a ticket,

(j) double entry means responsive to a sequential double entry ticket issuing machine comprising

(i) means for first causing an interrogation signal to first cause the generation of a first particular transaction signal associated with the first of the entries and the generation of a second interrogation signal to cause the generation of a second particular transaction signal associated with the second entry,

(ii) means for storing said first particular entry signal, and

(iii) means for activating said generating means only after said first and second particular transaction signals are generated;

(5) testing means for testing for an inequality of the storage address signals generated by said first and second transaction processing means to transmit an ambiguity signal to said deactivating means, comprising

(a) means responsive to an erroneous-transaction indicating signal from the checking means of either of said first and second transaction processing means for disabling said inequality testing means,

(b) means responsive to erroneous-transaction indicating signals from both of said first and second transaction processing means for transmitting a joint error signal to said deactivating means;

(6) a ticket issuing machine memory comprising

(a) a plurality of addressed memory positions each storing the number of transactions made by a ticket issuing machine,

(b) address-selection means for receiving the portion of the storage address signals generated by the master transaction processing means for selecting the particular memory position associated with the ticket issuing machine being interrogated,

(c) reading means for reading out the contents of the selected memory position,

(d) updating means for updating the read-out contents, and

(e) returning means for returning the updated contents to the selected memory position;

(7) a third pair of units consisting of first and second concurrently operating transaction calculating means each comprising

(a) register means having

(i) addressed aggregation registers for storing the aggregations of transactions processed by only the master transaction processing means, and

(ii) other registers for storing operation and result information,

(b) means responsive to the storage address signals generated by said generating means for selecting the addressed aggregation registers represented by the storage address signals,

(c) means for reading out the contents of said selected addressed aggregation register,

(d) means for updating the contents of said selected addressed aggregation register,

(e) means for returning said updated contents to said selected addressed aggregation register,

(f) means for generating an acknowledgment signal which is transferred to the acknowledgment signal responsive means of the interrogated ticket issuing machine when said updated contents are returned to said selected addressed aggregated register, and

(g) a computer for operating on said aggregated transactions to obtain result information, said computer comprising

(i) means for checking for errors in the calculations for transmitting an erroneous-transaction indicating signal to said console means so that if the master transaction calculating means transmitted said signal, said master selecting means selects the slave transaction calculating means to be the master transaction calculating means, and

(ii) means under the control of said master selecting means for transferring the result information as output information from the master transaction calculating means;

(8) means for testing for an inequality of the result information of said computers for transmitting an ambiguity signal to said deactivating means comprising

(a) means responsive to an erroneous-transaction indicating signal from the computer error checking means of either the first or second transaction calculating means for disabling said computer inequality testing means; and

(b) means responsive to erroneous-transaction signals from both of said first and second transaction calculating means for transmitting a joint error signal to said deactivating means;

(9) information display means for receiving and displaying the output information transferred from said master transaction calculation means; and

(10) means for preventing the reinterrogating of a ticket issuing machine which has received an acknowledgement signal or a rejection signal until the bid signal generated by said ticket issuing machine terminates.

While the system has been described for single entry and

3,252,149

daily double transactions, it can easily be modified to handle other multiple entry transactions such as parlays and quinellas in animal racing parlance.

Furthermore, although the processing of a daily double transaction has been described as being performed by two consecutive scan arounds to the same ticket-issuing machine it is equally possible on one scan to interrogate the ticket issuing machine twice to process the transaction before stepping off to the next ticket issuing machine.

It should also be noted that such a system can not only be employed locally to service a single track for all transactions made at that track but can also be employed to service ticket issuing machines located at "off track" installations. Furthermore, the system can be employed to service a plurality of tracks simultaneously both for "on track" and "off track" betting transactions. In such a case, multientry transactions such as parlays need not be restricted to only animals running at the same track.

While only one embodiment of the invention has been shown and described in detail, it will now be apparent to those skilled in the art that many modifications and variations may be made which do not depart from the appended claims.

What is claimed is:

1. A data processor for processing transaction signals comprising:

(A) a plurality of pairs of units, each unit of each pair performing the same function as the other unit but with one operating as a master unit and the other as a slave unit,

(B) a master selecting means for selecting which unit of each pair of units is a master and which is a slave and for changing the selection upon receipt of an erroneous-transaction indicating signal only from the selected master unit, and

(C) checking means responsive to transaction signals being processed in each unit of a pair of units for checking for erroneous transaction signals and for transmitting an erroneous-transaction indicating signal to said master selecting means so that if the master unit caused said erroneous-transaction signal, said master selecting means then selects the slave unit to be the master unit.

2. In a system which comprises a plurality of machines wherein each of said machines comprises a plurality of selectable signal generators for transmitting a selected transaction signal to an associated output line, a data processor for processing transaction signals comprising:

(A) a plurality of pairs of units, each unit of each pair performing the same function as the other unit but with one operating as a master and the other as a slave,

(B) a master selecting means for determining which unit of each pair of units is a master and which is a slave and for changing the selection upon receipt of an erroneous-transaction indicating signal from the selected master unit,

(C) connecting means for connecting said master and slave units respectively to the output lines of said machines for concurrently processing said particular transaction signals, and

(D) checking means responsive to transaction signals being processed in each unit of a pair of units for checking for erroneous transaction signals and for transmitting an erroneous-transaction indicating signal to said master selecting means so that if the master unit caused said erroneous-transaction signal, said master selecting means selects the slave unit to be the master unit.

3. In a system which comprises a plurality of machines wherein each of said machines comprises a plurality of switches for transmitting a selected transaction signal to an associated output line, a data processor for processing transaction signals comprising:

(A) a plurality of pairs of units, each unit of each pair performing the same function as the other unit but with one operating as a master and the other as a slave, and

(B) a master selecting means for determining which unit of each pair of units is a master and which is a slave and for changing the selection upon receipt of an erroneous-transaction indicating signal from the selected master unit,

(C) one pair of units comprising first and second transaction processing means each connected respectively to the output lines of said machines for concurrently processing said selected transaction signals,

(D) each of said transaction processing means including checking means responsive to transaction signals being processed in its associated transaction processing means for checking for erroneous transaction signals and for transmitting an erroneous-transaction indicating signal to said master selecting means so that if the master transaction processing means transmitted said signal, said master selecting means then selects the slave transaction processing means to be the master transaction processing means.

4. The apparatus of claim 3 further comprising another pair of units consisting of first and second concurrently operating transaction calculating means each comprising

(A) addressed aggregation registers for storing the aggregations of transactions, and

(B) a computer for operating on said aggregated transactions to obtain result information, said computer comprising error checking means for checking for errors in the calculations for transmitting an erroneous-transaction indicating signal to said master selecting means so that if the master transaction calculating means transmitted said signal, said master selecting means selects the slave transaction calculating means to be the master transaction calculating means.

5. The apparatus of claim 4 wherein said first and second concurrently operating transaction calculating means are each responsive only to processed transaction signals transmitted from the master transaction processing means.

6. The apparatus of claim 4 further comprising another pair of units consisting of first and second scanning means each comprising

(A) interrogating means for simultaneously interrogating sequentially and periodically each of said machines to determine if it is to perform a transaction as indicated by an operated switch, and

(B) transmitting means for transmitting to the operated switch an interrogated signal from only the scanning means selected by said master selecting means to be the master scanning means.

7. The apparatus of claim 6 wherein said computer further comprises

(A) transferring means under control of said master selecting means for transferring the result information as output information from the master transaction calculating means, and

(B) information display means for receiving and displaying the output information transferred from said master transaction calculating means.

8. The apparatus of claim 7 further comprising first and second pluralities of buffer means, each of said buffer means of each of said pluralities having

(A) one input line connected to one of the associated output lines of each machine, and

(B) one output line connected to one of the first and second transaction processing means.

9. The apparatus of claim 3 wherein each of said first and second transaction processing means further comprises synchronizing means for synchronizing processing steps between said first and second transaction processing means comprising

(A) means for transmitting a process step-finished signal from one to the other transaction processing means when a processing step is finished, and

(B) means responsive to the simultaneous presence of process step-finished signals from both transaction processing means for enabling said transaction processing means to proceed to the next step.

10. The apparatus of claim 1 further comprising
(A) testing means for simultaneously testing the output data of a pair of units and producing an ambiguity signal when said output data is unequal, and
(B) deactivating means for deactivating the data processor in response to an ambiguity signal.

11. The apparatus of claim 4 further comprising
(A) first testing means for simultaneously testing the processed data from said first and second transaction processing means and producing an ambiguity signal when said processed data is unequal,
(B) second testing means for simultaneously testing the result information produced by said first and second transaction calculating means and producing an ambiguity signal when said result information is unequal, and
(B) deactivating means responsive to an ambiguity signal for deactivating the system.

12. The apparatus of claim 4 wherein each of said transaction processing means further comprises
(A) generating means for generating storage address signals representing the selected transaction and the particular machine under interrogation, and
(B) means responsive to the storage address signals generated by said generating means for selecting the addressed aggregation registers.

13. The apparatus of claim 12 wherein said first and second transaction calculating means each further comprises
(A) means for reading out the contents of the selected addressed aggregation register,
(B) means for updating the contents of said selected addressed aggregation register,
(C) means for returning said updated contents to said selected addressed aggregation register, and
(D) means for transmitting an acknowledgement signal to the master transaction processing means when said updated contents are returned to said selected addressed aggregation register.

14. The apparatus of claim 9 further comprising means responsive to an erroneous-transaction indicating signal from said checking means for disabling said synchronizing means.

15. The apparatus of claim 10 further comprising means responsive to an erroneous-transaction indicating signal from said checking means for disabling said testing means.

16. The apparatus of claim 11 further comprising means responsive to an erroneous-transaction indicating signal for disabling said first testing means if said signal is transmitted by the checking means of either transaction processing means and for disabling said second testing means if said signal is transmitted by the error-checking means of either transaction calculating means.

17. The apparatus of claim 1 further comprising
(A) means responsive to erroneous-transaction signals from each unit of a pair of units for producing a joint error signal, and
(B) deactivating means responsive to a joint error signal for deactivating the data processor.

18. The apparatus of claim 4 further comprising
(A) means responsive to erroneous-transaction indicating signals from both of said first and second transaction processing means for producing a joint error signal,
(B) means responsive to erroneous-transaction indicating signals from both of said first and second transaction calculating means for producing a joint error signal, and
(C) deactivating means responsive to a joint error signal for deactivating the system.

19. The apparatus of claim 3 wherein each of said machines also comprises a rejection device for rejecting a transaction, said apparatus further comprising means responsive to an erroneous-transaction indicating signal transmitted from said checking means for operating said rejection device.

20. A system comprising
(A) a plurality of ticket issuing machines wherein each of said ticket issuing machines comprises
(1) a plurality of selectively actuatable and latching transaction-selection switches each associated with a different entry in a race for transmitting a selected transaction signal associated with the selected entry,
(2) an acknowledgement signal responsive means for issuing a ticket having indica recorded thereon which is related to a latched switch,
(B) generating means responsive to said selected transaction signal for generating signals representing the entry associated with the particular transaction signal and representing the particular ticket issuing machine, and
(C) transaction calculating means for performing a calculation on said generated signals and transmitting an acknowledgement signal to said acknowledgement signal responsive means for issuing a ticket only if the transaction is correct.

21. The system of claim 20 wherein said transaction calculating means comprises
(A) register means having addressed aggregation registers for storing the aggregations of transactions,
(B) means responsive to the signals generated by said generating means for selecting the addressed aggregation register,
(C) means for reading out the contents of said selected addressed aggregation register,
(D) means for updating the contents of said selected addressed aggregation register,
(E) means for returning said updated contents to said selected addressed aggregation register, and
(F) means for transmitting said acknowledgement signal to the acknowledgement signal responsive means when said updated contents are returned to said selected addressed aggregation register.

22. The system of claim 20 further comprising a ticket issuing machine memory comprising
(A) a plurality of addressed memory positions each storing the number of transactions made by a ticket issuing machine,
(B) address-selection means for receiving the signals generated by said generating means for selecting the particular memory position associated with the particular ticket issuing machine,
(C) reading means for reading out the contents of the selected memory position,
(D) updating means for updating the read-out contents, and
(E) returning means for returning the updated contents to the selected memory position.

23. A system comprising
(A) a plurality of ticket issuing machines wherein each of said ticket issuing machines comprises
(1) a plurality of selectively actuatable and latching transaction-selection switches each associated with a different entry in a race for transmitting a selected transaction signal associated with the selected entry,
(2) a rejection signal responsive means for unlatching any latched switches,
(3) and an acknowledgement signal responsive means for issuing a ticket having indicia recorded thereon which is related to a latched switch,

(B) switch means which comprises a plurality of selectively actuatable transaction-prevention switches for generating non-allowed signals associated with entries upon which transactions will not be allowed,
(C) comparing means for comparing the selected transaction signal with the nonallowed signals to generate a nontransaction signal when a particular transaction signal and a nonallowed signal represent the same entry,
(D) rejection means responsive to a nontransaction signal from said comparing means for transmitting a rejection signal to the rejection signal responsive means of the ticket issuing machine for unlatching any latched switches, and
(E) means for transmitting an acknowledgement signal to the acknowledgement signal responsive means of the ticket issuing machine for issuing a ticket only if the selected transaction is allowed.

24. A system comprising:
(A) a plurality of ticket issuing machines each including a plurality of selectively actuatable transaction selection switches each associated with a different entry for transmitting when actuated a selected entry transaction signal associated with a selected entry to an output line when the ticket issuing machine receives an interrogation signal,
(B) scanning means for sequentially and periodically selecting each of the ticket issuing means for interrogation,
(C) interrogating means for generating an interrogation signal for transmission to the selected ticket issuing machine,
(D) sensing means for sensing for a selected entry transaction signal, and
(E) means for stepping said scanning means to the next ticket issuing machine when said sensing means does not sense a selected entry transaction signal.

25. The system of claim 24 further comprising means for processing a selected entry transaction signal sensed by said sensing means before the stepping of said scanning means to select the next ticket issuing machine.

26. A system comprising:
(A) a ticket issuing machine which comprises
(1) a plurality of selectively actuatable and latching transaction-selection switches each associated with a different entry for transmitting a selected entry transaction signal associated with the selected entry to an associated output line,
(2) a rejection signal responsive means for unlatching any latched switches upon receipt of a rejection signal, and
(3) an acknowledgement signal responsive means for issuing a ticket having indicia recorded thereon which is related to a latched switch,
(B) entry checking means for checking for erroneous selected entry transaction signals and for transmitting a rejection signal to said ticket issuing machine when erroneous selected entry transaction signals are sensed, and
(C) means for transmitting acknowledgement signals to said ticket issuing machine when the selected entry transaction signal is correct.

27. The system of claim 26 wherein said entry checking means comprises means for sensing for the simultaneous presence of more than one selected entry transaction signal.

28. The system of claim 26 wherein said ticket issuing machine transmits a selected entry transaction signal only in response to an interrogating signal, said system further comprising interrogating means for producing interrogating signals, said checking means further comprising means for sensing for the presence of a selected entry transaction signal when the interrogating signal is not present.

29. A system comprising:
(A) a plurality of ticket issuing machines each including
(1) a plurality of selectively actuatable and latching transaction selection switches each associated with a different entry for transmitting when latched a selected transaction signal associated with a selected entry when the ticket issuing machine receives an interrogation signal,
(2) means for generating a bid signal as long as any one of the transaction selection switches is latched, and
(3) acknowledgement signal responsive means for issuing a ticket having indicia recorded thereon which is related to the selected entry and for unlatching any latched transaction selection switches,
(B) scanning means for sequentially and periodically selecting each of the ticket issuing means for interrogation,
(C) interrogating means for generating an interrogation signal for transmission to the selected ticket issuing machine,
(D) means for processing the selected transaction signal and for generating an acknowledgement signal for transmission to the selected ticket issuing machine to issue said ticket and unlatch any latched transaction selection switches, and for stepping said scanning means to select the next ticket issuing machine, and
(E) means for preventing said interrogating means from transmitting an interrogating signal to a ticket issuing machine which has received an acknowledgement signal until the termination of the bid signal.

30. The system of claim 29 further comprising
(A) sensing means for sensing for a selected transaction signal, and
(B) means for stepping said scanning means to select the next ticket issuing machine when said sensing means does not sense a selected transaction signal.

31. A system for recording a multientry transaction related to one entry selected from each of two groups of entries comprising:
(A) transaction signal generation means for generating a first entry transaction signal representing the entry selected from the first group of entries and a second entry transaction signal representing the second entry selected from the second group of entries,
(B) storage means responsive to said transaction signal generation means for storing the first entry transaction signal,
(C) address generation means responsive to said transaction signal generation means and said storage means for generating a storage address signal related to the first and second entry transaction signals, and
(D) addressed storage registers responsive to said address generation means for storing the multientry transaction in the particular addressed storage register represented by the storage address signals generated by said address generation means.

32. The system of claim 31 further comprising:
(A) interrogation means for sequentially interrogating said transaction signal generating means, and transaction selection means for first selecting the first entry transaction for interrogation and then selecting the second entry transaction for interrogation,
(B) said storage means being only responsive to said transaction signal generation means when said transaction selection means selects the first entry transaction.

33. The system of claim 32 wherein said address generation means is responsive to said transaction selection means to generate a storage address signal only after said

transaction selection means selects the second entry transaction.

References Cited by the Examiner

UNITED STATES PATENTS

2,345,212	3/1944	Nelson	235—92
3,029,414	4/1962	Schrimpf	340—172.5
3,034,714	5/1962	Helsel et al.	235—92
3,047,223	7/1962	Lange	235—92
3,051,384	8/1962	Lange	235—92
3,061,192	10/1962	Terzian	235—157

FOREIGN PATENTS

749,836	6/1956	Great Britain.

OTHER REFERENCES

Pages 4-1 to 4-4, November 1949, Functional Description of the EDVAC, published by the University of Pennsylvania, Vol. 1.

Pages 101-107, December 1959, Chao: The System Organization of MOBIDIC, Proceedings of the Eastern Joint Computer Conference, No. 16.

Pages 33-78, 1961, Gass: Project Mercury Real-Time Computational and Data Flow System, Proceedings of the 1961 Eastern Joint Computer Conference. Vol. 20. QA 76 E3 C.9.

ROBERT C. BAILEY, *Primary Examiner.*

MALCOLM A. MORRISON, *Examiner.*

P. J. HENON, *Assistant Examiner.*

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

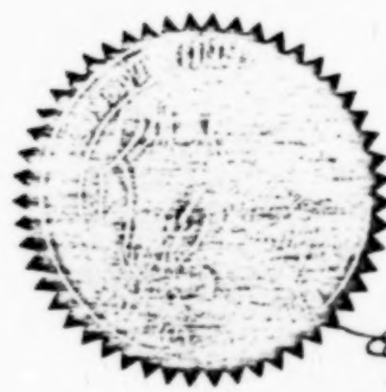
Patent No. 3,252,149 May 17, 1966

Robert L. Weida et al.

It is certified that error appears in the above identified patent and that said Letters Patent are hereby corrected as shown below:

In the drawings, Figure 1A, change "FTA" to -- TFA --; Figure 1A, change "FTB" to -- TFB --; Figure 1A, change "M2B" to -- HNB --; Figure 2, delete the line connected between line "SADD" and element "AATA"; Figure 2, insert a line connecting line "SADD" and element "WATA"; Figure 2, insert a line connecting line "AADRB" and element "WATA"; Figure 2, change "FTA" to -- TFA --; Figure 2, change "FTB" to -- TFB --; Figure 3, the line DD1 connected to gate A41 should read -- DD1′ --. Column 1, line 28, after "pairs" insert -- of --; line 51, "a more versatile system. Briefly, in view of this" should read -- a high speed scanning means for interrogating --. Column 3, line 32, "this signal such as the BID1′ signal." should read -- the signal such as the BID1 signal. However, --; line 49, after "not" insert -- the SCN1B signal from --; line 59, "preset" should read -- presets --. Column 6, line 62, "REJF" should read -- REJAF --. Column 8, line 34, "A14" should read -- A16 --; line 41, "CONFA" should read -- CONAF --. Column 9, line 62, "BNA" should read -- NA --. Column 10, line 28, "ERA" should read -- ERA′ --; line 31, "ERA′" should read -- ERA --. Column 12, line 19, "barrel" should read -- barred --. Column 13, line 73, "CERA" should read -- ERCA --. Column 15, line 36, "convention" should read -- conventional --. Column 16, line 15, "units" should read -- unit --. Column 17, line 67, cancel the period and insert -- , comprising --.

Signed and sealed this 16th day of December 1969.



William E. Schuyler, Jr.

WILLIAM E. SCHUYLER, JR.
Commissioner of Patents

Attest:

Edward M. Fletcher, Jr.

Attesting Officer